(14)

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-107216
(43)Date of publication of application : 24.04.1998

(51)Int.Cl.	H01L 27/10 H01L 27/04 H01L 21/822 H01L 27/108 H01L 21/8242 H01L 21/8247 H01L 29/788 H01L 29/792 H01L 41/08 H01L 49/00

(21)Application number : 08-262697
(22)Date of filing : 03.10.1996

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(54) COMPOSITE STRUCTURE OF CRYSTALLINE OXIDE DIELECTRIC THIN FILM AND SINGLE CRYSTAL SILICON SUBSTRATE, ELECTRONIC DEVICE USING THE SAME, AND MANUFACTURE OF THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To realize an IS structure having a crystalline oxide dielectric layer having little leak current, a high breakdown voltage, and a sufficiently long life with the elapse of time against the breakdown voltage, that is, a composite structure of a crystalline oxide dielectric thin film and a single crystal silicon substrate.
SOLUTION: In a composite structure in which a crystalline oxidc dielectric thin film 2 is grown on a single crystal silicon semiconductor substrate 1, the crystalline oxide dielectric thin film 2 is formed by a thin film (single film or stacked layer made of, for example, stabilized zirconia, cerium oxide, strontium titanate, magnesium oxide, or yttrium oxide) to which a heat treatment is performed in an active oxygen atmosphere after the growth.

LEGAL STATUS

[Date of request for examination]	30.01.2003
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（A）　(11)特許出願公開番号

特開平10－107216

(43)公開日　平成10年(1998)４月24日

(51)Int.Cl.[6]		識別記号	FI		
H01L	27/10	451	H01L	27/10	451
	27/04			49/00	Z
	21/822			27/04	C
	27/108			27/10	651
	21/8242			29/78	371

審査請求　未請求　請求項の数10　ＯＬ　（全 15 頁）　最終頁に続く

(21)出願番号　特願平8－262697

(22)出願日　平成８年(1996)10月３日

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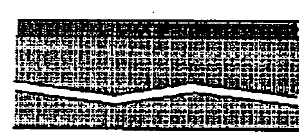
(54)【発明の名称】　結晶性酸化物誘電体薄膜と単結晶シリコン基体との複合構造体およびそれを用いた電子素子およびそれらの製造方法

(57)【要約】

【課題】リーク電流が少なく、絶縁破壊耐圧が高く、経時的絶縁破壊寿命が充分長い結晶性酸化物誘電体層を有するＩＳ構造、すなわち結晶性酸化物誘電体薄膜と単結晶シリコン基体との複合構造体を実現する。

【解決手段】単結晶シリコン半導体基体１に結晶性酸化物誘電体薄膜２を成長させた複合構造体において、前記結晶性酸化物誘電体薄膜２を、成長後に活性酸素雰囲気で熱処理を施された薄膜（例えば安定化ジルコニア、酸化セリウム、チタン酸ストロンチウム、酸化マグネシウム、酸化イットリウムの何れかからなる単層膜または積層膜）で形成した複合構造体。

（図１）



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【特許請求の範囲】

【請求項１】単結晶シリコン半導体基体に結晶性酸化物誘電体薄膜を成長させた複合構造体において、

前記結晶性酸化物誘電体薄膜が、成長後に活性酸素雰囲気で熱処理を施された薄膜であることを特徴とする結晶性酸化物誘電体薄膜と単結晶シリコン基体との複合構造体。

【請求項２】単結晶シリコン半導体基体に結晶性酸化物誘電体薄膜を成長させた複合構造体を含む電子素子において、

前記複合構造体が、その形成後から電子素子構造を完成させるまでの間に少なくとも１回、活性酸素雰囲気で熱処理を施された薄膜であることを特徴とする電子素子。

【請求項３】前記結晶性酸化物誘電体薄膜が前記単結晶シリコン基体にヘテロエピタキシャル成長させた単結晶膜であることを特徴とする請求項１に記載の複合構造体または請求項２に記載の電子素子。

【請求項４】前記結晶性酸化物誘電体薄膜が複数の材料の積層によって形成された多層膜からなることを特徴とする請求項１乃至請求項３の何れかに記載の複合構造体または電子素子。

【請求項５】前記結晶性酸化物誘電体薄膜が安定化ジルコニア、酸化セリウム、チタン酸ストロンチウム、酸化マグネシウム、酸化イットリウムから選ばれた一つあるいは複数の材料によって構成された単層膜あるいは積層膜であることを特徴とする請求項１乃至請求項４の何れかに記載の複合構造体または電子素子。

【請求項６】上記電子素子は、単結晶シリコン半導体基体（Ｓ）の一部に、順に結晶性酸化物誘電体薄膜（Ｉ）と強誘電体薄膜（Ｆ）と金属電極膜（Ｍ）を積層し、該積層膜の非形成部の少なくとも一部にソース電極とドレイン電極とを設けたＭＦＩＳトランジスタであり、

該結晶性酸化物薄膜が、成長後もしくは強誘電体薄膜成長後に、少なくとも１回、活性酸素雰囲気で熱処理を施された薄膜であることを特徴とする請求項２乃至請求項５の何れかに記載の電子素子。

【請求項７】上記電子素子は、単結晶シリコン半導体基体（Ｓ）の上に一つまたは複数の結晶性酸化物誘電体薄膜（Ｉ）と単結晶シリコン膜をエピタキシャル成長させたＳＯＩ基板であり、

該結晶性酸化物薄膜が、その成長後に、少なくとも１回、活性酸素雰囲気で熱処理を施された薄膜であることを特徴とする請求項２乃至請求項５の何れかに記載の電子素子。

【請求項８】前記活性酸素雰囲気での熱処理が、酸素を供給しながら１９０ｎｍ未満の波長を含む紫外線照射下で熱処理する方法、オゾンを供給しながら熱処理する方法、酸素プラズマ下で熱処理する方法、のいずれか一つの方法、あるいは二つ以上の方法を組合せて同時に行なう方法、あるいは二つ以上の方法を異なった時点で重複して行なう方法によって達成されることを特徴とする請求項１乃至請求項７の何れかに記載の複合構造体または電子素子の製造方法。

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【請求項９】前記活性酸素雰囲気での熱処理が結晶性酸化物誘電体薄膜形成直後に実施されることを特徴とする請求項１乃至請求項８の何れかに記載の複合構造体または電子素子の製造方法。

【請求項１０】前記活性酸素雰囲気での熱処理が結晶性酸化物誘電体薄膜を形成し、該結晶性酸化物誘電体薄膜の上に導電性酸化物、あるいは、酸化物半導体膜、酸化物超電導体膜、酸化物強誘電体膜の少なくとも一つを形成した後に施されることを特徴とする請求項２乃至請求項８の何れかに記載の電子素子の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、リーク電流の極めて少ない結晶性の酸化物誘電体薄膜と単結晶シリコン（Ｓｉ）基板との複合構造体とこれを利用した電子素子の構造、ならびにこれら構造体や電子素子の製造方法に関する。なお、ここで言う結晶性誘電体薄膜とは単結晶または特定の方向に優先配向した誘電体薄膜を意味するものとする。

【０００２】

【従来の技術】単結晶膜は、一般に、アモルファス膜や多結晶膜に比べて、結晶構造的に平坦かつ均一なため、導電性、誘電性、絶縁性、強誘電性、超電導性、半導体特性、光透過性、光磁気特性、結晶周期性等のその材料特有の物理的諸特性が強く鋭く現れるという特長を有している。そのため、様々な工業分野で有用であり、その実現が強く望まれている。近年、これら単結晶膜をＳｉ半導体素子や集積回路に積載して、従来のＳｉ系材料だけでは達成できない付加価値の高い集積回路やスマートデバイスを実現しようとする試みが活発に行われるようになってきいる。このような新規なＳｉ半導体デバイスを構成する上で欠かせない基本構造が結晶性の誘電体薄膜（Ｉ）と単結晶Ｓｉ（Ｓ）との複合構造体（以下ＩＳ構造体と略称）である。

【０００３】一例を挙げると、図８の模式的構造断面図に示すようなＭＦＩＳ型不揮発性ランダムアクセスメモリセルがある。このセルは金属（Ｍ）－シリコン酸化膜（Ｏ）－半導体（Ｓ）からなるＭＯＳトランジスタのＯ部分を、電気的に反転可能な自発分極をもつ単結晶強誘電体膜（Ｆ）と単結晶誘電体膜（Ｉ）とで置き換えたものである。

【０００４】図８において、１０１はｐ型の（１００）面の単結晶Ｓｉ基板、１０２はＳｉ基板１０１上にヘテロエピタキシャル成長された単結晶酸化物誘電体膜（Ｉ）であり、たとえば（１００）面のＹＳＺ膜である。１０３は単結晶酸化物誘電体膜１０２の上にヘテロエピタキシャル成長された強誘電体膜であり、たとえば

（００１）面のＰｂＴｉO_3膜である。１０４は強誘電体膜１０３上に形成されたゲート電極であり、たとえばＰｔ電極である。１０５および１０６はｎ型のソース電極およびドレイン電極であり、それぞれＰ（リン）やＡｓ（ヒ素）をイオン注入して、熱拡散で活性化させて形成したものである。

【０００５】このメモリでは、ゲート電極（Ｇ）－Ｓｉ基板（Ｓｕｂ）間に正または負のパルス電圧を印加して、強誘電体膜の自発分極ベクトルを反転固定させ、トランジスタを導通あるいは非導通状態にさせることで情報の記録を行う。

【０００６】また、上記の強誘電体層としては、化学的気相成長法（ＣＶＤ）やマグネトロンスパッタリング法などで形成されたＰｂＴｉO_3（チタン酸鉛）膜やＰｂ（Ｚｒ$_x$, Ｔｉ$_{1-x}$）O_3（ジルコンチタン酸鉛）膜、Ｂｉ$_4$Ｔｉ$_3O_{12}$（チタン酸ビスマス）膜など（いずれも分極軸配向単結晶膜）が検討されている。

【０００７】また、上記の単結晶誘電体層としては、電子ビーム蒸着法やＣＶＤで形成されたＣｅO_2（酸化セリウム）膜やＹＳＺ（イットリヤ安定化ジルコニヤ）膜、ＳｒＴｉO_3（チタン酸ストロンチウム）膜などが検討されている。これらの単結晶誘電体膜は単結晶強誘電体膜を形成するためのテンプレート層として機能するほかに、強誘電体とＳｉ基板が相互拡散するのを防止する緩衝層としての役割を担っている。

【０００８】また、不揮発性ランダムアクセスメモリセルには、上記のＭＦＩＳ構造の他に、ＭＦＭＩＳ構造も提案されている。ここで単結晶Ｆ層と単結晶Ｉ層の間に挿入されたＭ層は単結晶の導電膜、たとえばＰｔ膜などである。この場合もＭＦＭ構造の下部にＩＳ構造体が用いられる。

【０００９】次に、図９の模式的構造断面図に示したＳＯＩ構造のＭＯＳトランジスタもＩＳ構造体の重要な応用例である。この構造のＭＯＳトランジスタは動作上極めて有害なラッチアップ現象から完全に免れることができるという特筆すべき特徴がある。

【００１０】図9において、１１１は（１００）面のＳｉ基板、１１２は該Ｓｉ基板１１１に接してヘテロエピタキシャル成長されたＣｅO_2やＹＳＺ、ＳｒＴｉO_3などの単結晶誘電体膜である。このＳｉ基板１１１と単結晶誘電体膜１１２とがＩＳ構造を成している。１１３は単結晶誘電体膜１１２上にＣＶＤでヘテロエピタキシャル成長されたｐ型の（１００）面の単結晶Ｓｉ層、１１４は単結晶Ｓｉ層１１３の熱酸化で形成されたＳｉO_2ゲート酸化膜、１１５はゲート酸化膜１１４の上にＣＶＤとドライエッチングで形成されたポリシリコンのゲート電極である。１１６および１１７はN形のソース電極およびドレイン電極であり、それぞれＰ（リン）やＡｓ（ヒ素）をイオン注入して、熱拡散で活性化させて形成したものである。

【００１１】また、集積回路の高速化処理を目指して試みられている酸化物高温超電導薄膜配線などでもＩＳ構造体の上に高品質の単結晶超電導体膜（たとえばＹＢａ$_2$Ｃｕ$_3O_7$）配線を形成する。Ｉ層としては、たとえば、ＹＳＺとＹ$_2O_3$の単結晶積層膜が用いられる。

【００１２】このようにＩＳ構造体は、単結晶の機能性薄膜（強誘電体膜、半導体膜、導電膜、超電導膜、誘電体膜）を含有する様々なデバイスを単結晶Ｓｉ基板上で実現するための重要な基本構造であることが理解される。しかし、現状では単結晶酸化物誘電体薄膜Ｉ層に、（１）リーク電流が大きい、（２）破壊強度が低い、（３）経時破壊（ＴＤＤＢ）寿命が短い、という問題があり、上述のような高機能デバイスの実現に大きな障害となっている。

【００１３】上記の問題を実際のデータに基づいて詳しく説明する。図７は結晶性酸化物誘電体薄膜のリーク電流特性図である。図７において、特性曲線（ａ）は従来の単結晶ＹＳＺ膜の特性例を示すものであり、N型単結晶（１００）面のＳｉ基板にエピタキシャル成長させた（１００）面のＹＳＺ膜に、直径２００［μｍ］のＡｌ電極（ゲート）を形成して作製したＭＩＳ容量のゲート電極に、正の電圧を印加して測定したリーク電流密度Ｊ［Ａ／ｃｍ^2］を、電界強度Ｅｏｘ［Ｖ／ｃｍ］の関数として示したものである。なお、吸収電流成分を除くために、電流の測定は、電圧印加してから充分時間が経過した後に行っている。また、膜厚は４０［ｎｍ］であり、成膜法は、ここでは電子ビーム蒸着法である。基板の洗浄法ならびに成膜法（蒸着条件等）は本発明の実施例の中で後述する。

【００１４】図７の特性曲線（ａ）を見てわかるように、従来例の単結晶ＹＳＺ膜のリーク電流は非常に高い水準にある。実用を考えると、リーク電流密度は電界強度Ｅｏｘ＝１［ＭＶ／ｃｍ］のとき、Ｊ＝１［ｎＡ／ｃｍ^2］以下に抑制したい。しかし、上記の従来例ではＪ＝１００［μＡ／ｃｍ^2］台と、これと大きくかけ離れた値を示している。また、図７の特性曲線（ａ）におけるＡ点の電流ジャンプは、この電圧（Ｅｏｘ≒１．５［ＭＶ／ｃｍ］）でＹＳＺ膜が絶縁破壊をしていることを示している。前述のＭＦＩＳ不揮発性メモリセルなどに適用するには、この絶縁破壊強度は充分とは言えない値である。

【００１５】さらにＩ層には、電源ストレスに対する長期的な絶縁破壊（ＴＤＤＢ）耐性があることが必須の条件である。この耐性は一般に誘電体膜に定電流ストレスを与え、絶縁破壊するまでに膜を通過した総電荷量Ｑｂｄ［Ｃ／ｃｍ^2］を測定して評価する。上記の単結晶ＹＳＺ膜に、Ｊ＝０．１［ｍＡ／ｃｍ^2］の定電流ストレスを与えた時の典型的なＴＤＤＢ寿命は、それぞれＱｂｄ＝１．２［ｍＣ／ｃｍ^2］であった。この値はＭＯＳトランジスタなどのゲート酸化膜として用いられている熱酸

化ＳｉＯ$_2$膜の代表的な値Ｑｂｄ～１０［Ｃ／ｃｍ^2］と並べると比べようもなく低い。電源ストレスが比較的強いＭＦＩＳ不揮発性メモリセルなどにＹＳＺ膜を適用するには、少なくとも０．１［Ｃ／ｃｍ^2］台のＴＤＤＢ寿命が必要である。

【００１６】ＩＳ構造におけるこのようなＩ層の問題は、電子ビーム蒸着法で形成した単結晶ＹＳＺ膜に限ったことではなく、他の単結晶酸化物誘電体材料膜や他の成膜法で作製したＹＳＺ膜でも共通して観察される問題である。

【００１７】

【発明が解決しようとする課題】本発明は、このような従来のＩＳ構造体およびこれを用いたデバイスの結晶性誘電体膜（Ｉ層）の問題点を解決するためになされたものであり、リーク電流が少なく、絶縁破壊耐圧が高く、経時的絶縁破壊寿命が充分長い結晶性酸化物誘電体層を有するＩＳ構造、すなわち結晶性酸化物誘電体薄膜と単結晶シリコン基体との複合構造体およびそれを用いた電子素子およびそれらの製造方法を実現することを目的としている。

【００１８】

【課題を解決するための手段】上記目的を達成するために、本発明においては、ＩＳ複合構造体およびこれを用いた電子素子およびそれらの製造方法を各特許請求の範囲に記載しているように構成した。すなわち、請求項１に記載の発明においては、単結晶シリコン半導体基体に結晶性酸化物誘電体薄膜を成長させたＩＳ複合構造体において、Ｉ層は成長後に活性酸素雰囲気で熱処理を施した結晶性酸化物誘電体薄膜であるとした。

【００１９】同様に請求項２においては、ＩＳ複合構造体を含み、これの上に構築された電子素子において、Ｉ層は成長後から電子素子を完成させるまでの間に活性酸素雰囲気で熱処理（以下活性酸素アニールと称する）を施された結晶性酸化物誘電体薄膜であるとした。

【００２０】請求項３～５は請求項１または請求項２の具体的な態様を示したものである。すなわち請求項３においては、結晶性酸化物誘電体薄膜を単結晶シリコン基体にヘテロエピタキシャル成長させた単結晶膜で構成している。また、請求項４においては前記結晶性酸化物誘電体薄膜を複数の酸化物誘電体膜の積層によって形成される多層膜によって構成している。また、請求項５においては結晶性酸化物誘電体薄膜が安定化ジルコニア、酸化セリウム、チタン酸ストロンチウム、酸化マグネシウム、酸化イットリウムから選ばれた単層膜あるいは積層複合膜であるとしている。

【００２１】また、請求項６および請求項７は、電子素子の具体的態様を示すものであり、請求項６は電子素子がＭＦＩＳトランジスタ（ＭＦＩＳ型不揮発性ランダムアクセスメモリセル）の場合、請求項７は電子素子がＳＯＩ（Silicon On Insulater）基板である場合を示す。

【００２２】さらに、請求項８は前記請求項に記載の複合構造体あるいは電子素子の製造方法であって、製造工程中にあって結晶性酸化物誘電体薄膜の活性酸素アニールは、酸素を供給しながら１９０ｎｍ未満の波長を含む紫外線照射下で熱処理する方法、オゾンを供給しながら熱処理する方法、酸素プラズマ下で熱処理する方法、のいずれか一つの方法、あるいは二つ以上の方法を組合せて同時に行なう方法（例えば紫外線照射下でオゾンを供給しながら熱処理する）、あるいは二つ以上の方法を異なった時点で重複して行なう方法（一つの方法を行なった後に次の方法を行なう）によって達成される。なお、上記紫外線の波長１９０ｎｍ未満とは、酸素を分解して活性酸素とする能力を有する範囲を意味する。

【００２３】また、請求項９は、製造方法の一態様であって、活性酸素雰囲気での熱処理が結晶性酸化物誘電体薄膜形成直後に実施されるものである。また、請求項１０は、前記電子素子の製造方法の一態様であって、活性酸素雰囲気での熱処理が結晶性酸化物誘電体薄膜を形成し、該結晶性酸化物誘電体薄膜の上に導電性酸化物、あるいは、酸化物半導体膜、酸化物超電導体膜、酸化物強誘電体膜の少なくとも一つを形成した後に施されるものである。

【００２４】以下、作用について説明する。まず、単結晶Ｓｉ基板上に形成した結晶性酸化物薄膜のリーク電流の機構について説明する。本発明者が鋭意研究して明らかにしたところによると、結晶性酸化物薄膜のリーク電流の原因には、（１）酸化物の結晶粒内部の酸素空位、（２）結晶粒内部の金属元素ボイド、（３）結晶粒界面のエネルギー準位、（４）結晶粒間隙の金属Ｓｉ元素、などがあり、各原因に基づいて（分離はできないが）異なるリーク電流が流れる。上記の原因（１）と（２）は結晶の格子点にあるべき原子が確率的に抜けてしまういわゆる点欠陥である。金属元素が抜けるとこれと結合している酸素原子も一緒に抜けることが多く、金属－酸素ボイドとなる。これら点欠陥は酸化物の禁止帯に電子準位を形成し、この密度が一定以上になると準位間を容易に電子が移動できるようになり、所謂ホッピング電導を引き起こす。このような点欠陥はアモルファス膜でもしばしば観察され、やはりリーク電流の原因になっている。

【００２５】上記の原因（１）、（２）が粒界内を流れるリーク電流の原因であったのに対して、原因（３）と（４）は粒界面を流れるリーク電流に関するものであり、結晶性酸化膜特有の原因である。ここで単結晶Ｓｉにエピタキシャル成長している結晶性酸化物薄膜に“粒界”とは、奇異な印象を受けかもしれないが、これは格子定数が微妙に違う異種材料を単結晶Ｓｉにヘテロエピタキシャル成長させるとき、ヘテロ面の格子不整ストレスを開放するために必然的に生じる粒界であり、成長面に垂直方向に粒界面が延びている。この粒界面では結晶

周期が中断し、粒界面に存在する原子のなかには、化学結合していないものが多数存在する。上記の原因（３）はこれら未結合原子が存在する結果として結晶性酸化物禁制帯内部に形成された電子準位である。電子準位が高濃度になるとバンドを形成しリーク電流を増大させる。原因（４）は結晶性酸化物薄膜の成膜時にＳｉ基板から侵入し結晶粒界に偏析した金属Ｓｉ原子である。結晶粒界には１～数原子層程度の空隙があるので、減圧下（低酸素濃度下）成長時に基板から侵入してきたＳｉは金属状態（または低価数状態）のまま粒界間隙にトラップされる。粒界に偏析したＳｉは当然、リーク電流の導電経路になる。

【００２６】リーク電流の発生のメカニズムを説明し終えたところで、本発明がリーク電流を含む従来の問題を如何にして解決するか（作用）について説明する。本発明者の最近の研究成果によると、本発明によるリーク電流の低減はつぎのような機構に基づいて起こると考えられる。本発明の活性酸素アニールでは、反応性の高いＯ（^{1}Ｄ）やO_2（^{1}Δｇ）、Ｏ（^{3}Ｐ）などの活性酸素が気相で豊富に発生している雰囲気で結晶性酸化物薄膜／単結晶Ｓｉ構造体を比較的低温で熱処理する。このとき活性酸素はＳｉ基板に向かって内方拡散する。活性酸素の一部は原因（１）の酸素空位に遭遇し、空位を消滅（充填）させて安定する。また活性酸素の他の一部は粒界に向かって、あるいは、粒界に沿って拡散し、粒界に偏析している金属状シリコンを酸化してSiO_2とし、粒界間隙部をSiO_2ネットワークで満たす。これによって原因（４）の金属Ｓｉが除去される。なお、上記の熱処理温度は、常温から約５００℃程度までの範囲とし、特に２００～５００℃程度が望ましい。その理由は５００℃以上の高温では活性酸素が通常の酸素に変わってしまい、また、２００℃以下ではアニール時間が長くなるためである。

【００２７】さらに、結晶粒界面に存在していた未結合手原子Ｍは粒界間隙にSiO_2ネットワークが形成される過程で、近接するＳｉとＭ－Ｏ－Ｓｉ結合を成し、その未結合手を解消する。これによって原因（３）が解消される。残りの活性酸素は単結晶Ｓｉ基板まで拡散し、結晶性酸化物薄膜／Ｓｉ界面に極めて薄いSiO_2膜を成長させる。SiO_2の成長は一般に体積の膨張を伴うが、熱処理温度が低温である活性酸素アニールでは、通常の熱酸化のように圧縮応力に打ち勝って成長するのは困難であるから、活性酸素アニールでは一部のＳｉ元素を酸化物膜中に放出し、体積の膨張を押えながら界面での酸化が進行する。ここで放出されたＳｉ原子は外方拡散する過程で金属－酸素ボイドに遭遇し、金属原子位置に捕獲される。一方、このとき気相からは活性酸素が内方拡散しており、ボイドに捕獲されたＳｉ原子に遭遇することが可能であり、ボイドに近接する酸化物の複数の金属とＳｉ原子との中間に入ってＭ－Ｏ－Ｓｉ結合を完成させる。こうして原因（２）の金属－酸素ボイドはＳｉ－O_x（ｘ＝４～５）原子団によって補填され、消滅する。なお、ボイドに捕獲されなかった大多数のＳｉ原子は酸化物薄膜の表面に析出する。この析出物は結晶性酸化物薄膜上への他の薄膜のエピタキシャル成長を阻害するので、本発明においては成長前に弗酸溶液などで除去される。

【００２８】こうして本発明の構造ならびに方法によれば、リーク電流の上記原因（１）～（４）をすべて除去することができる。この結果、本発明は実施例にて後述するように、従来例に比べ、結晶性酸化物薄膜のリーク電流を数桁のレベルで低減することができる。

【００２９】つぎに本発明による絶縁破壊強度ＢＥｏｘやＴＤＤＢ寿命を示す総電荷量Ｑｂｄの改善について述べる。本発明の対象とするCeO_2やＹＳＺなどの結晶性酸化物薄膜の絶縁破壊や疲労のメカニズムは、研究段階にあり十分に解明されているとは言い難い。しかし、電界強度Ｅｏｘや総電荷量Ｑｂｄとリーク電流Ｊとの間には強い正の相関があることは広く認められている。これは、ＥｏｘやＱｂｄを決定する要因とリーク電流の原因とが共通していることを示唆している。本発明は上述のように結晶性酸化物のリーク電流の原因を除去することができるから、これと深く関わる絶縁破壊や疲労の要因を取り除くことができ、結果として、従来例に比べて、絶縁破壊強度ＢＥｏｘを高く、総電荷量Ｑｂｄを大きくすることができる。

【００３０】

【発明の効果】以上説明してきたように本発明においては、結晶性酸化物誘電体薄膜と単結晶Ｓｉ基板との複合構造体において、該結晶性誘電体薄膜を成長後に活性酸素アニールを施した膜としたため、結晶性誘電体膜における（１）リーク電流特性、（２）絶縁破壊強度、（３）経時的絶縁破壊（ＴＤＤＢ）耐性、を改善することができるという効果が得られる。

【００３１】また本発明においては、結晶性酸化物誘電体膜と単結晶Ｓｉ基板との複合構造体を含む電子素子に上記本発明による複合構造体を適用することにより、上記（１）～（３）の特性不良に起因して生じていた電子素子の破壊や動作不良を解消できるという効果が得られる。

【００３２】

【発明の実施の形態】以下、本発明にかかる結晶性酸化物誘電体薄膜と単結晶Ｓｉ基板との複合構造体と、該複合構造体を含む電子素子と、複合構造体および電子素子の製造方法を、実施の形態および実施例に基づいて説明する。

【００３３】（実施の形態）図１は本発明に基づく結晶性酸化物誘電体薄膜と単結晶Ｓｉ基板との複合構造体の一実施の形態を示す断面図である。図１において、１は（１００）、（１１１）、（１１０）面などの所定の結

晶面を有する単結晶Ｓｉ基板、２は、電子ビーム蒸着法、イオンビームスパッタリング法、分子線エピタキシー法、レーザアブレーション法などの物理的気相成長法やＣＶＤなどの化学的気相成長法にてＳｉ基板１上にヘテロエピタキシャル成長された結晶性酸化物誘電体薄膜、あるいは単結晶酸化物誘電体薄膜である。これに該当する誘電体薄膜としては、Y_2O_3やSm_2O_3、ＣａＯなどで安定化されたジルコニア膜（たとえばＹＳＺ膜）、酸化セリウム（CeO_2）膜、チタン酸ストロンチウム（$SrTiO_3$）膜、酸化イットリウム（Y_2O_3）膜、酸化マグネシウム（ＭｇＯ）などが挙げられるが、これに限定されるものではなく、Ｓｉ基板にヘテロエピタキシャル成長される酸化物誘電体薄膜なら他の薄膜でもよい。酸化物誘電体薄膜２は、Ｓｉ基板１に成長された後、Ｓｉ基板１とともにO_3やO（^1P）、O（^1D）、O_2（$^1\Delta g$）、O^{2-}などの活性酸素雰囲気の中で常温から５００［℃］未満の温度で所定時間、熱処理を施される。こうして本発明に基づく複合構造体が完成する。

【００３４】以下に、上記の本発明複合構造体の実施の形態の具体的な実施例を提示するとともに、これを作製する工程を示すことによって本発明の製造方法の実施例も併せて説明することにする。

【００３５】（実施例１）本発明に基づく複合構造体の最初の具体的な実施例は（１００）面の単結晶Ｓｉ基板１とエピタキシャル成長された（１００）面の単結晶イットリヤ安定化ジルコニア（ＹＳＺ）薄膜２とからなる複合構造体を、高真空電子ビーム蒸着法とＵＶ／O_2活性酸素アニールとを用いて構築する例である。ここでＵＶは活性酸素の生成手段としての紫外線を意味し、O_2は活性酸素の原料としての酸素を意味する。

【００３６】はじめに、（１００）面の単結晶Ｓｉ基板１の表面の汚染物および自然酸化物を、ＲＣＡ洗浄（ア＊＊ンモニア水と過酸化水素水の混合液による洗浄と、塩酸と過酸化水素水の混合液による洗浄からなる伝統的なＳｉ基板洗浄法）と希フッ酸洗浄（５％濃度のＨＦ水溶液に数１０秒浸漬した後、純水でリンスし乾燥する洗浄法）とで除去する。

【００３７】つづいてＳｉ基板１上に約１３モル％のY_2O_3を含有するＹＳＺ膜を高真空電子ビーム蒸着法にて形成する。蒸着機は実験用あるいは量産用として市販されている汎用の高真空型の装置である。蒸着のターゲットは単結晶ＹＳＺ（$Y_2O_3$１３ｍｏｌ％）インゴットを直径１５ｍｍ、厚み７ｍｍの切削加工したＹＳＺタブレットである。

【００３８】成膜の手順を説明すると、蒸発源にＹＳＺタブレットを充填し、洗浄したＳｉ基板１を蒸着槽の基板ホルダに設置して、速やかに蒸着槽内を排気する。基板ホルダは基板を常温から１０００［℃］までの温度に加熱する能力を有しており、蒸着源とは３０［ｃｍ］の距離を隔てて対抗している。蒸着装置の排気は強力であり、内部の圧力は10^{-9}［Ｔｏｒｒ］以下まで減圧することが可能である。蒸着槽の圧力が10^{-6}［Ｔｏｒｒ］に達したら基板温度を加熱して所定の成膜温度にする。温度が安定し、かつ、蒸着槽内の圧力が10^{-9}［Ｔｏｒｒ］以下に下がったところで高速の電子ビームをタブレットに射突させ、０．２［ｎｍ／ｍｉｎ］の成長速度でＹＳＺ膜をＳｉ基板に成長させる。ＹＳＺの膜厚が概ね３［ｎｍ］になったところで外部から蒸着槽に高純度乾燥酸素を導入して圧力を2×10^{-6}［Ｔｏｒｒ］に調節するとともに成長速度を５［ｎｍ／ｍｉｎ］に上げ、所定の膜厚になるまで成長を続ける。成長速度は熱陰極の放出電流を制御して調節する。（１００）面の単結晶ＹＳＺ薄膜が得られる典型的な成膜条件は次のとおりである。

【００３９】

ＹＳＺ成膜条件

成膜圧力	1×10^{-8}［Ｔｏｒｒ］（膜厚３ｎｍまで）
	2×10^{-6}［Ｔｏｒｒ］（膜厚３ｎｍからO_2導入）
成膜温度	８００［℃］（基板温度）
ターゲット	Y_2O_3：ZrO_2＝１３：８７
基板距離	３０ｃｍ
電子ビーム加速電圧	８ｋＶ

膜厚が所望の値になったところで蒸着電源の出力を切って成膜を終える。この後、蒸着槽に基板を置いたまま基板を徐冷し、基板温度が十分低くなってから基板を蒸着槽から取出す。このようにして堆積したＹＳＺ膜はホタル石構造（立方晶）を有する単結晶エピタキシャル膜であった。

【００４０】従来例として前に説明したＹＳＺ薄膜と単結晶Ｓｉとの複合構造体は、ここまでの工程で完成となる。しかし、本発明に基づく複合構造体ではこの後、活性酸素アニール工程を実施する。ここでは活性酸素アニールのひとつ、ＵＶ／O_2アニールの例で説明するが、後述の他の活性酸素アニールでも構わない。

【００４１】図２は、アニールに使用する装置の模式的要部断面図である。図２において、１１は側壁が水冷されている反応器、１２は反応器１１を排気するための真空ポンプで、反応器１１の圧力を常圧から10^{-6}［Ｔｏ

ｒｒ］までの間に維持することができる。１３は単結晶Ｓｉ基板に単結晶ＹＳＺ薄膜を成長したアニール前の複合構造体である。１４は１３を支持し所定の温度に保持するためのサセプタである。複合構造体１３はサセプタ１４上にＹＳＺ膜面が上に向くように置かれている。１５は純度９９．９９９％以上の酸素O_2を充填したガスボンベである。アニールに際して、ボンベのO_2は整圧器１６で0．５［ｋｇ／ｃｍ^2］程度の圧力に減圧された後、質量流量調節器１７で所定の流量に調節され、反応器１１に導かれる。１８はキセノンガスが封入された誘電体バリア放電エキシマランプで、中心波長１７２［ｎｍ］の強力な紫外光ＵＶを発生することができる。エキシマランプ１８から出射された紫外励起線は合成石英窓１９を通して反応器１１内部に入射される。２０は反応器１１と真空ポンプ１２を結ぶ排気配管を開閉する排気バルブ、２１は大気排出バルブである。なお、上記紫外光の波長は酸素を分解して活性酸素とする能力を有する範囲の値であり、一般に１９０ｎｍ未満であることが必要である。

【００４２】次のような手順でＵＶ／O_2アニールを行＊う。所定の温度に加熱されているサセプタ１４の上に複合構造体１３を載せ、真空ポンプ１２を作動させると同時に、排気バルブ２０を開口し、直ちに反応器１１内を真空排気する。内部の圧力が１０$^{-5}$［Ｔｏｒｒ］台に到達したところで排気バルブ２０を閉口し、真空ポンプ１２を停止し、高純度O_2ガスを反応器１１に１０００［ｃｃ／ｍｉｎ］程度の質量流量で導入する。反応器の内圧が常圧（＝大気圧）になったところで、大気排出バルブ２１を開口し、以降導入される余剰なO_2ガスを所定の質量流量で反応器１１外に排出する。こうすることによって反応器１１を大気圧の純酸素雰囲気に維持することができる。つづいてエキシマランプ１８から反応器１１内部に紫外励起線を出射する。反応器１１内部に入射した１７２［ｎｍ］波長の紫外光は反応器１１内のO_2に強く吸収され、結果として、O_3やO（^{3}P）、O（^{1}D）、O_2（$^1\Delta g$）、などからなる活性酸素が発生する。以上の準備が整ったところで、ＵＶ／O_2活性酸素アニールを所定の時間、実施する。典型的なアニール条件を下に示す。

＊【００４３】

活性酸素アニール（ＵＶ／O_2）条件

容器圧力	大気圧
処理温度	３５０［℃］
励起強度（合成石英ガラス位置）	１３［mW／ｃｍ^2］（１７２［ｎｍ］）
O_2流量	２００［ｃｃ／ｍｉｎ］
処理時間	１５［ｍｉｎ］

アニールが終了したら、エキシマランプ１８の出射と高純度O_2の導入を停止し、直ちに複合構造体１３を取り出す。こうして、ＵＶ／O_2アニールが終わり、本発明の結晶性酸化物誘電体薄膜と単結晶Ｓｉ基板との複合構造体が完成する。

【００４４】なお、上記の処理温度（アニール温度）は、常温から約５００℃程度までの範囲とし、特に２００～５００℃程度が望ましい。実験結果によると５００℃以上の高温では活性酸素が通常の酸素に変わってしまい、また、２００℃以下ではアニール時間が長くなる。

【００４５】次に、本発明の実施例の効果を従来例の実測データと対比させながら説明する。図７の特性曲線（ｂ）は、上記実施例１に基づいて作製したＹＳＺ／Ｓｉ基板の複合構造体において、ＹＳＺ膜の上にＡｌゲート電極を蒸着して形成したＭＩＳ容量に正の電圧を印加して測定したリーク電流（ＹＳＺ膜に流れる電流）特性を示している。なお、特性曲線（ａ）は従来例による複合構造体のリーク特性（既述）である。

【００４６】図７の特性曲線（ａ）と（ｂ）を比較すれば、本発明の実施例が従来例に比べてリーク電流を概ね４桁～５桁低減させていることが分かる。Ｅｏｘ＝１［MV／ｃｍ］の特性を見ると、従来例が電流密度Ｊ＝１００［μＡ／ｃｍ^2］台なのに対し、本発明の実施例ではＪ＝１［ｎＡ／ｃｍ^2］以下の値を与えている。

【００４７】次に絶縁破壊強度ＢＥｏｘに着目すると、測定によれば、従来例ではＢＥｏｘ＝1．5［MV／ｃｍ］であったが、本発明実施例ではＢＥｏｘ＝4．6［MV／ｃｍ］と３倍以上の向上が見られた。

【００４８】また、定電流ストレス0．1［mA／ｃｍ^2］を与えた時のＴＤＤＢ寿命は、従来例が総電荷量Ｑｂｄ＝1．2［mC／ｃｍ^2］であった（既述）のに対して、本発明の実施例ではＱｂｄ＝８５０［mC／ｃｍ^2］の値であって、３桁近い改善が得られた。

【００４９】以上の結果から、本発明が、結晶性酸化物薄膜／Ｓｉ基板の複合構造体における結晶性酸化物薄膜の、（１）リーク電流の低減、（２）絶縁破壊強度の向上、（３）ＴＤＤＢ寿命の増長、に極めて有効であることが理解される。

【００５０】（実施例２）本発明に基づく複合構造体の２番目の具体的な実施例は、（１００）面の単結晶Ｓｉ基板とエピタキシャル成長させた（１１０）面の単結晶酸化セリウム（ＣｅO_2）薄膜２とからなる複合構造体を、高真空電子ビーム蒸着法とＵＶ／O_3活性酸素アニールとを用いて形成する例である。ここで「／O_3」は

8％のオゾンO_3を含む原料としての酸素を意味する。

【0051】はじめに、n型の（100）面の単結晶Si基板の表面の汚染物および自然酸化物をRCA洗浄と希フッ酸洗浄とで除去する。つづいてSi基板上にCeO_2薄膜を高真空電子ビーム蒸着法にてピタキシャル成長させる。蒸着機は前記YSZ成長で用いた装置と同じものを用いる。蒸着ターゲットは純度99.999％以上のCeO_2粉末をホットプレスで直径15［mm］、厚み7［mm］の形に成形したしたタブレットである。蒸発源にCeO_2タブレットを充填し、Si基板を蒸着槽の基板ホルダに設置し、蒸着槽内を排気する。蒸着槽の圧力が10^{-6}［Torr］に達したら基板温度を加熱＊して所定の成膜温度にする。温度が安定し、槽内圧力が10^{-9}［Torr］以下に下がったところで高速の電子ビームをタブレットに射突させ0.4［nm／min］の成長速度でCeO_2膜を成長させる。膜厚が概ね5［nm］になったところで蒸着槽に高純度乾燥酸素を導入して圧力を8×10^{-6}［Torr］に調節するとともに成長速度を1.55［nm／min］に上げ、所定の膜厚になるまで成長を続ける。成長速度は熱陰極の放出電流を制御して調節する。上記（110）面の単結晶CeO_2薄膜が得られる典型的な成膜条件は次のとおりである。

【0052】

（110）面のCeO_2成膜条件

成膜圧力	1×10^{-8}［Torr］以下（膜厚3［nm］まで）
	8×10^{-6}［Torr］（膜厚3［nm］からO_2導入）
成長温度	800［℃］（基板温度）
ターゲット	純度99.999％CeO_2タブレット
基板距離	30cm
電子ビーム加速電圧	8kV

所望の膜厚になったところで蒸着電源の出力を切って成膜を終える。このようにして堆積したCeO_2膜はホタル石構造（立方晶）を有する（110）面の単結晶エピタキシャル膜であった。ちなみに、同じ（100）面のSi基板上に配向方向が異なる（111）面の単結晶CeO_2膜を得ることも可能である。この場合には、上記成長条件において、成長温度を600［℃］とする。従来例はこの段階で完成となる。本発明に基づく複合構造体ではこの後、活性酸素アニール「UV／O_3アニール」工程を実施する。

【0053】図3はアニールに使用する装置の模式的要部断面図である。図2と同じ番号を付した部位の機能・構成は図2と同じであるので、冗長を避け、説明を省略する。図3において、31は工程途上のCeO_2／Si複合構造体である。整圧器16と質量流量計17の間には無声放電型のオゾン発生器32が設置されている。このオゾン発生器32は酸素を原料に8モル％のO_3を発生することができる。33は低圧水銀ランプで、波長185［nm］と254［nm］に強い輝線をもつ紫外光を発生することができる。低圧水銀ランプ33から出射された紫外励起線は合成石英窓19を通して反応器11内部に入射される。

【0054】UV／O_3アニールの手順は前述のUV／O_2アニールとほぼ同じである。すなわち所定温度のサセプタ14の上に構造体31を載せ、直ちに反応器11内を真空排気する。反応器11内部の圧力が10^{-5}［Torr］台に到達したところで排気バルブ20を閉口し、真空ポンプ12を停止し、高純度O_2ガスを反応器11に1000［cc／min］程度の質量流量で導入する。反応器11の内圧が常圧（＝大気圧）になったところで、大気排出バルブ21を開口すると同時にオゾン発生器32を作動させて8％のO_3を含む高純度O_2ガスを反応器11に導入する。間を置かず低圧水銀ランプ33から反応器11内部に紫外励起線を出射する。反応器11内部に入射した254［nm］の紫外光は器内のO_3を光分解し、結果として、O_3のほかに$O(^1D)$、$O_2(^1\Delta g)$、$O(^3P)$などからなる活性酸素が発生する。こうして、UV／O_3活性酸素アニールを所定の時間、実施する。典型的なアニール条件は次のとおりである。

【0055】

活性酸素アニール（UV／O_3）条件

容器圧力	大気圧
処理温度	400［℃］
励起強度（合成石英ガラス位置）	20［mW／cm^2］（254［nm］）
O_2流量	200［cc／min］
処理時間	60［min］

アニールが終了したら、低圧水銀ランプ３３の出射とオゾン発生器３２の作動、高純度O_2の導入を停止し、直ちに複合構造体を取り出す。こうして、本発明による結晶性酸化物誘電体薄膜と単結晶Ｓｉ基板との複合構造体が完成する。

【００５６】次に、本実施例２の効果を説明する。下記の表１は本実施例２ならびに従来例に基づくCeO_2／＊Ｓｉ複合構造体のCeO_2薄膜（２０［ｎｍ］）の電界強度１［ＭＶ／ｃｍ］におけるリーク電流ＪＬ、絶縁破壊強度ＢＥｏｘ、定電流０．１［ｍＡ／ｃm^2］を与えたときのＴＤＤＢ寿命（総電荷量Ｑｂｄ）を比較した表である。

【００５７】

【表１】

（表１）

CeO_2／Ｓｉ複合構造体の電気特性の比較

	リーク電流ＪＬ［ｎＡ／ｃm^2］	絶縁破壊強度ＢＥox［ＭＶ／ｃｍ］	総電荷量Ｑｂｄ［ｍＣ／ｃm^2］
実施例	０．４５	５．１	１８００
従来例	３５００	１．４	１２．４

【００５８】上記表１の電気特性は前記実施例１と同様にＭＩＳ容量（Ａｌゲート）に正の電圧を印加して測定した。表１から明かなとおり、本発明の実施例２は従来例に比べてリーク電流ＪＬを概ね４桁低減し、絶縁破壊強度ＢＥｏｘを３．５倍向上させている。さらにＴＤＤＢ寿命に対応する総電荷量Ｑｂｄを１Ｃ／ｃm^2台に乗せ、ＴＤＤＢ寿命を従来よりも２桁向上させることに成功した。以上の結果から、本発明の実施例２が、結晶性酸化物薄膜／Ｓｉ基板の複合構造体における結晶性酸化物薄膜のリーク電流や絶縁破壊強度、ＴＤＤＢ寿命の改善に効果的であることは明白である。

【００５９】なお、上記活性酸素アニールにおいて、ＵＶを用いないアニール、すなわちO_3アニールに置き換えることも可能である。O_3アニールも活性酸素を生じるので有効である。熱処理装置の構成はＵＶ／O_3より簡単になるが、熱処理時間がＵＶを用いたときに比べて２倍程度のびる。また、前述実施例や後述の実施例の他の活性酸素アニール法も用いることができる。

【００６０】（実施例３）本発明に基づく複合構造体の３番目の具体的な実施例は（１００）面の単結晶Ｓｉ基板１と（００１）面の単結晶チタン酸ストロンチウム（ＳｒＴｉO_3）薄膜２とからなる複合構造体をレーザアブレーション蒸着法とｐｌａｓｍａ／O_2アニールで形成する例である。

【００６１】ｎ型の（１００）面の単結晶Ｓｉ基板の表面の汚染物および自然酸化物をＲＣＡ洗浄と希フッ酸洗浄とで除去した後、Ｓｉ基板上にＳｒＴｉO_3薄膜を高真空レーザアブレーション蒸着法にて成長する。蒸着機は真空中で切り替え可能な２個の蒸着源を備えている汎用機である。各々の蒸着源には純度９９．９９９％以上の粉末をホットプレスで円盤状（１０φ、１０ｔ）に整形したＳｒＯタブレットとＳｒＴｉO_3タブレットが充填されている。

【００６２】成長の手順を説明すると、前記洗浄直後のＳｉ基板１を蒸着槽中の基板ホルダに設置し、蒸着槽内を排気する。このホルダは基板を常温から８００［℃］までの温度に加熱する能力を有しており、タブレットから約５［ｃｍ］の距離を挟んで対抗している。蒸着装置の排気は強力であり、内部の圧力は10^{-9}［Ｔｏｒｒ］以下まで背圧を下げることが可能である。蒸着槽の圧力が10^{-8}［Ｔｏｒｒ］に達したところで基板ホルダを加熱して所定の成長温度にする。温度が安定するまでの間に、ＳｒＯが充填されている第１の蒸発源を使用する準備を行う。

【００６３】蒸着槽内の圧力が10^{-8}［Ｔｏｒｒ］以下に下がったところでレーザ光源の出力をオンして高密度のレーザ光をタブレットに射突させ、非常に薄いＳｒＯバッファ膜の成長を開始する。本実施例のレーザはＫｒＦ（波長２４８ｎｍ、パルス幅２０ｎｓ）エキシマレーザである。繰り返し周波数は１０［Ｈｚ］、エネルギー密度は１．０［Ｊ／ｃm^3］であった。ＳｒＯバッファ膜の厚みが６［ｎｍ］になったところでレーザの出力を停止して、成長を止める。直ちに蒸発源をＳｒＴｉO_3タブレットが収められている第２の蒸発源に切り替えるとともに、基板ホルダの温度をＳｒＴｉO_3成長に適した所定の温度に変更する。温度が安定したところで、外部から高純度酸素を導入し、圧力を5×10^{-5}［Ｔｏｒｒ］とし、再びレーザの出力をオンして今度はＳｒＴｉO_3膜を成長させる。膜厚が所望の値になったところでレーザ光源の発信を停止し、O_2の導入を止め、基板を

徐冷する。単結晶（００１）面のＳｒＴｉO_3膜が得られる成長条件の一例をまとめると次のとおりである。

【００６４】

ＳｒＯバッファ膜の成長条件

成長圧力	１×１０$^{-8}$［Ｔｏｒｒ］以下
成長温度	８００［℃］（基板温度）
タブレット－基板距離	５［ｃｍ］
レーザ光源	ＫｒＦエキシマレーザ（エネルギー１３０ｍＪ）
励起パルス	幅２０ｎｓ、繰り返し周波数１０Ｈｚ

ＳｒＴｉO_3膜の成長条件

成長圧力	５×１０$^{-5}$［Ｔｏｒｒ］（９９．９９９％酸素導入）
成長温度	６００［℃］（基板温度）
他の条件は上のＳｒＯと同じ	

基板温度が十分低くなってから基板を蒸着槽から取出す。最初に形成した６［ｎｍ］のＳｒＯ層は後のＳｒＴｉO_3膜を成長する過程で消失する（ＳｒＴｉO_3膜に変質したと考えられる）ので、こうして形成した膜は事実上単結晶ＳｒＴｉO_3単層膜である。

【００６５】従来例はこの段階の構成で完成である。本発明に基づく複合構造体ではこの後、活性酸素アニールを行う。前出のＵＶ／O_2アニールやＵＶ／O_3アニールでも可能であるが、ここでは「ｐｌａｓｍａ／O_2アニール」の例を紹介する。

【００６６】図４はｐｌａｓｍａ／O_2アニールに使用する装置の模式的要部断面図である。図４において、４１は側壁が水冷されている反応器、４２は反応器４１を排気するための真空ポンプで、反応器４１の圧力を常圧から１０$^{-6}$［Ｔｏｒｒ］までの間に維持することができる。４３はアニール前の複合構造体である。４４は複合構造体４３を支持し所定の温度に保持する加熱手段を備えたサセプタである。このサセプタ４４は電気的に接地されている。複合構造体４３はＳｒＴｉO_3膜面が上に向くようにサセプタ４４に置かれる。サセプタ４４と対抗するように置かれているのがパワー電極４５である。パワー電極４５はブロッキング容量４６と整合器４７を介して器外の高周波電源４８（例えば周波数１３．５６ＭＨｚ）に電気的に接続されている。４９は純度９９．９９９％以上の酸素O_2を充填したガスボンベである。ガスボンベ４９のO_2は整圧器５０で０．５［ｋｇ／ｃｍ^2］程度の圧力に減圧された後、質量流量調節器５１で所定の流量に調節され、反応器４１に導かれる。５２は反応器４１と真空ポンプ４２を結ぶ排気配管を開閉する排気バルブ、５３は反応器の圧力を一定に制御する圧力制御バルブである。

【００６７】ｐｌａｓｍａ／O_2アニールの手順は次のとおりである。所定の温度に加熱されているサセプタ４４の上に処理前の複合構造体４３を載せ、真空ポンプ４２を作動させると同時に、排気バルブ５２を開口し、直ちに反応器４１内を真空排気する。反応器４１内部の圧力が１０$^{-5}$［Ｔｏｒｒ］台に到達したところで高純度O_2ガスを反応器４１に所定の質量流量で導入するとともに圧力制御バルブ５３を作動させて、反応器４１の内圧を所定の値に調節する。内圧とサセプタ温度が安定するまで待ってから、高周波電源４８の出力をオンし、サセプタ４４とパワー電極４５との間で放電を起こさせ、アニールを開始する。放電が起こると、O_3やＯ（^{3}Ｐ）、Ｏ（^{1}Ｄ）、O_2（$^1\Delta g$）、などからなる活性酸素が発生する。以上の準備が整ったところで、ＵＶ／O_2活性酸素アニールを所定の時間、実施する。典型的なアニール条件を下に示す。

【００６８】

活性酸素アニール（ｐｌａｓｍａ／O_2）条件

容器圧力	３［ｍＴｏｒｒ］
処理温度	４００［℃］
サセプターパワー電極間距離	３０［ｃｍ］
O_2流量	１［ｃｃ／ｍｉｎ］
高周波パワー	１００［Ｗ］
処理時間	２０［ｍｉｎ］

所定の時間が過ぎたらアニールを終了する。すなわち、高周波出力を停止し、圧力制御バルブ５３の作動を止め、排気バルブ５２を閉じ、真空ポンプ４２を停止し、反応器４１に空気を導入して大気開放し、複合構造体４

３を器外に取り出す。このようにして単結晶ＳｒＴｉO_3膜と単結晶Ｓｉ基板との複合構造体が完成する。

【００６９】次に本発明の実施例３の効果を説明する。下記の表２は実施例３ならびに従来例に基づくＳｒＴｉO_3／Ｓｉ複合構造体において、ＳｒＴｉO_3薄膜（４０ｎｍ）の電界強度１〔ＭＶ／ｃｍ〕におけるリーク電流＊ＪＬ、絶縁破壊強度ＢＥｏｘおよび定電流０．１〔ｍＡ／ｃm^2〕を与えたときの総電荷量Ｑｂｄを比較した表である。

【００７０】

【表２】

（表２）

ＳｒＴｉO_3／Ｓｉ複合構造体の電気特性の比較

	リーク電流ＪＬ〔ｎＡ／ｃｍ^2〕	絶縁破壊強度ＢＥox〔ＭＶ／ｃｍ〕	総電荷量Ｑｂｄ〔ｍＣ／ｃｍ^2〕
実施例	０．０８９	４．９	１３５０
従来例	２２０	２．３	８．１

【００７１】表２の電気特性は前記実施例と同様にＭＩＳ容量（Ａｌゲート）に正の電圧を印加して測定した。表２から判るように、実施例３においては、従来例に比べてリーク電流ＪＬを３桁強低減し、絶縁破壊強度ＢＥｏｘを２倍に向上させている。さらにＴＤＤＢ寿命に対応する総電荷量Ｑｂｄを３桁増大させ、Ｑｂｄを１〔Ｃ／ｃm^2〕台に乗せることに成功した。以上の結果は、本発明の実施例３が、結晶性酸化物薄膜／Ｓｉ基板の複合構造体における結晶性酸化物薄膜のリーク電流や信頼性の改善に大いに寄与し得る技術であることを示している。

【００７２】このような複合構造体の結晶性酸化物薄膜のリーク電流や信頼性を改善する効果は、ここまでの具体的実施例で説明したＹＳＺ膜やＣｅO_2膜、ＳｒＴｉO_3膜に限定されるものではなく、Ｓｉ単結晶基板に成長させた他の単結晶酸化物薄膜や配向性酸化物薄膜にも等しく現われる効果であり、本発明の適用範囲は広い。ただし、対象とする複合構造体に応じて活性酸素アニールの最適条件は異なる。

【００７３】また、結晶性酸化物薄膜の構成は説明の都合上、すべて単層膜としたが、異種の膜の積層膜でも同様の改善効果が得られる。たとえば、（００１）面のＣｅO_2単結晶膜と（００１）面のＳｒＴｉO_3単結晶膜を積層したＣｅO_2／ＳｒＴｉO_3／Ｓｉ複合構造体でも顕著なリーク軽減効果と絶縁破壊強度およびＴＤＤＢ耐性改善効果が現われる。

【００７４】次に、本発明を電子素子に適用した実施例について説明する。

（実施例４）本実施例は、前記図１に示したＩＳ複合構造体をＭＦＩＳ型不揮発性メモリセルに適用した例である。

【００７５】図５はＭＦＩＳ型不揮発性ランダムアクセスメモリセルの模式的構造断面図である。このセル構造は一見、前記図８で説明した従来のセル構造と同じであるが、結晶性酸化物誘電体薄膜Ｉが活性酸素アニールを施された膜であるところが、大きく異なっている。図５において、６１はｐ型の（１００）面の単結晶Ｓｉ基板、６２はＳｉ基板上に選択的に形成された厚いフィールド酸化膜で、このフィールド酸化膜６２が形成されていないところがモート領域６３である。メモリセルはこのモート領域６３に形成されている。６４はモート領域にヘテロエピタキシャル成長された単結晶酸化物誘電体膜（Ｉ）、たとえば（１００）面のＹＳＺ膜で、素子が完成するまでの間に活性酸素アニールを施された膜である。単結晶酸化物誘電体膜６４の上には強誘電体膜６５、たとえば（００１）面のＰｂＴｉO_3膜とゲート電極６６、たとえばＰｔ電極がある。強誘電体膜６５は結晶性酸化物誘電体薄膜６４の上にヘテロエピタキシャル成長している。６７、６８はｎ型不純物、たとえばＰやＡｓが高濃度にドープされているソース電極とドレイン電極である。

【００７６】次に、この素子の製造工程の要点を簡単に説明すると、初めにｐ型の（１００）面の単結晶Ｓｉ基板の表面の汚染物をＲＣＡ洗浄で除去した後、Ｓｉ基板前面に熱酸化法で４０〔ｎｍ〕の熱酸化膜を形成し、さらにその上に１５０〔ｎｍ〕のＳｉ$_3$Ｎ$_4$膜（以下ＳｉＮ膜と略記する）をＬＰＣＶＤ法で成膜する。つづいて、ホトリソグラフィとプラズマエッチング法を用いて、モート領域に相当する部分を残してＳｉＮ膜（および熱酸化膜）を除去する。次に、レジストを剥離し、再びＲＣＡ洗浄した後、熱酸化法（ＬＯＣＯＳ酸化）で４００〔ｎｍ〕のフィールド酸化膜を形成する。このとき、Ｓ

ｉＮ膜が形成されている部分には酸化膜は成長しないのでフィールド酸化膜と一緒にモート領域も形成される。この後、熱燐酸でＳｉＮ膜を除去する。

【００７７】つづいて、モート領域に単結晶（００１）面のＹＳＺ膜の成長を行う。ＲＣＡ洗浄と希弗酸洗浄とでモート領域の汚染物と自然酸化膜を除去したあと、基板全面に約１３モル％のY_2O_3を含有するＹＳＺ膜を２０［ｎｍ］、高真空電ビーム蒸着法にて成長する。この成膜については前述の複合構造体の実施例で説明したので、ここでは説明を繰り返さない。ＹＳＺ膜の成長が終わったあと、基板を１％濃度の稀弗酸に約１０秒浸漬さ＊せ、超純水でリンスし乾燥する。

【００７８】稀弗酸による洗浄が終わったところで、ＭＯＣＶＤ（有機金属気相成長）法を用いて（００１）面の単結晶ＰｂＴｉO_3の成長を行う。使用する原料はテトラエチル鉛〔Ｐｂ$(C_2H_5)_4$〕とテトライソプロポキシチタン〔Ｔｉ$(i-OC_3H_7)_4$〕と乾燥酸素（O_2）である。前二者は常温常圧で液体であり、いずれも気化器で気化し乾燥Ａｒキャリアガスで反応器に輸送する。成長装置は特別な装置ではなく汎用機を用いる。代表的な成膜条件は下記のとおりである。

【００７９】

（００１）面の単結晶ＰｂＴｉO_3のＭＯＣＶＤ成長条件

成長圧力	６〔Ｔｏｒｒ〕
成長温度	６４０〔℃〕（基板温度）
原　料	Ｐｂ$(C_2H_5)_4$，Ｔｉ$(i-OC_3H_7)_4$，O_2
気化温度	－１５℃〔Ｐｂ$(C_2H_5)_4$〕
	２５℃〔Ｔｉ$(i-OC_3H_7)_4$〕
ガス流量	
O_2	１００ｃｃ／ｍｉｎ
Ｐｂ原料キャリア（Ａｒ）	２５ｃｃ／ｍｉｎ
Ｔｉ原料キャリア（Ａｒ）	２２ｃｃ／ｍｉｎ
Ａｒ希釈	２００ｃｃ／ｍｉｎ

次に活性酸素アニール、たとえばＵＶ／O_3アニールを所定の時間実施する。ＵＶ／O_3アニールの詳細な説明はすでに述べているで省略する。この活性酸素アニールによって、先に成長したＹＳＺ膜ばかりではなくＰｂＴｉO_3強誘電体膜のリーク電流特性と絶縁破壊強度、ＴＤＤＢ耐性を同時に改善することができる。なお、活性酸素アニールをＹＳＺ膜形成の直後に行っても、無論良いが、この場合には強誘電体膜の電気特性の改善は望め※ない。

【００８０】強誘電体膜の成長を終了したら、次にゲート電極材料、たとえば白金Ｐｔの全面成膜を行う。Ｐｔの成膜は汎用のＤＣマグネトロンスパッタリング法を用いる。電極材料としては９９．９９％純度以上のＰｔターゲット、膜厚は１００［ｎｍ］厚である。Ｐｔの典型的なスパッタリング成膜条件は次のとおりである。

【００８１】

ＰｔのＤＣマグネトロンスパッタリング条件

成膜圧力	３［ｍＴｏｒｒ］
成膜温度	４００［℃］（基板温度）
原　料	９９．９９％Ｐｔターゲット
スパッタガス	Ａｒ
ターゲットー基板距離	３０［ｃｍ］
ＤＣパワー	１５０［Ｗ］

Ｐｔの成膜が済んだら、フォトリソグラフィとＡｒスパッタエッチング技術を用いてＰｔゲート電極を形成する。Ｐｔのエッチングが終了したレジストをそのままにして続けてＰｂＴｉO_3膜とＹＳＺ膜の反応性イオンエッチングを行う。エッチングガスはCF_4とO_2の混合ガスである。ＹＳＺ膜のエッチングが終了したら、レジストを灰化させて除き、基板表面の塵埃を有機溶剤を用いて超音波洗浄で除去する。

【００８２】つづいて、基板全面にＰをイオン注入する。Ｓｉ基板に注入されるのはモート領域のゲート電極を除く部分、すなわちソース、ドレイン領域である。加速電圧は１００［ｋｅＶ］、ドーズ量は5×10^{15}［個／cm^2］である。イオン注入が終了したら、ソース、ドレインの注入不純物の活性化を急速熱処理（ＲＴＡ）装置を用いて行う。熱処理温度は１２００［℃］、熱処理時間は３０秒である。このようにしてＭＦＩＳ型の強誘電体メモリセルが完成する。

【００８３】（実施例５）電子素子の他の実施例は、前

記本発明のＩＳ複合構造体を用いたＳＯＩ基板上にＭＯＳトランジスタを形成した例である。図６はＳＯＩ構造のＭＯＳトランジスタの模式的構造断面図である。この構造は図９で説明した従来例の構造と見かけ上、同じであるがＳｉエピタキシャル膜とＳｉ単結晶基板との間に挟持された結晶性酸化物誘電体薄膜が活性酸素アニールを施された膜であるところが、大きく異なっている。

【００８４】図６において、７１は高濃度に不純物ドープされたｎ形の（１００）面の単結晶Ｓｉ基板、７２はＳｉ基板７１上にヘテロエピタキシャル成長された単結晶酸化物誘電体膜（Ｉ）、たとえば（１００）面のＹＳＺ膜で、素子が完成するまでの間に活性酸素アニールを施された膜である。７３はＹＳＺ膜７２の上にヘテロエピタキシャル成長したｎ形またはｐ形の比較的厚い（１００）面の単結晶Ｓｉ膜である。７４は単結晶Ｓｉ膜７３上に形成された厚いフィールド酸化膜、７５はモート領域である。モート領域７５内にある７６はポリシリコンゲート電極であり、これと単結晶Ｓｉ膜７３との間にはSiO_2熱酸化膜（ゲート酸化膜）７７が形成されている。また７８、７９はｐ形またはｎ形の不純物が高濃度にドープされているソース電極とドレイン電極である。

【００８５】製造工程の要点を簡単に説明すると、初めに、高濃度にドープされたｎ形の（１００）面の単結晶Ｓｉ基板６１をＲＣＡ洗浄と稀弗酸洗浄とで表面を清浄にし、その全面に（００１）面のＹＳＺ膜を１５０［ｎｍ］、すでに説明した高真空電ビーム蒸着法にて成長させる。成長後、このＩＳ複合構造体に、前に説明した活性酸素アニール、例えば、ｐｌａｓｍａ／O_2アニールをやや長めに施す。このあと、基板を１％濃度の稀弗酸に約１０秒浸漬させ、超純水でリンスし乾燥する。つづいて（１００）面のＹＳＺ膜７２の表面に２μｍの厚みの（１００）面の単結晶Ｓｉを周知の常圧ＣＶＤ法でエピタキシャル成長させる。原料は$SiCl_4$とH_2である。このようにして低リーク電流、高絶縁破壊耐性のＳＯＩ基板ができる。

【００８６】次にエピタキシャルＳｉ膜全面にｐ形の不純物Ｂを3×10^{13}［個／cm^2］イオン注入し、基板表面をＲＣＡ洗浄で清浄にする。前出の実施例とまったく同じＬＯＣＯＳ酸化法でフィールド酸化膜７４とモート領域７５を形成する。ＬＯＣＯＳ酸化工程を経るあいだに先にイオン注入したＢ不純物はエピタキシャルＳｉ膜内に広く拡散しかつ活性化する。

【００８７】つづいて、基板を熱酸化してモート領域にゲート酸化膜となる薄いSiO_2熱酸化膜７７（厚み２０［ｎｍ］）を成長させ、さらにこの上にＬＰＣＶＤ法で膜厚３００［ｎｍ］のポリシリコン膜を堆積した後、フォトリソグラフィと反応性イオンエッチングを用いて、図６に示すように、ポリシリコンゲート電極７６を形成する。

【００８８】レジストを除去した後、基板表面にＰをイオン注入する。この注入でエピタキシャルＳｉ膜にＢが打ち込まれるのはモート領域のゲート電極を除く部分、すなわちソース、ドレイン領域である。ポリシリコンゲート電極にもＢが同時に打ち込まれる。加速電圧は１００［ｋｅＶ］、ドーズ量は5×10^{15}［個／cm^2］である。

【００８９】イオン注入が終了したら、基板表面をＲＣＡ洗浄で清浄にした後、ソース電極７８、ドレイン電極７９、ゲート電極７６の不純物を活性化するために、１１２０［℃］に加熱した拡散炉内で２時間のドライブインを行う。このようにして本発明に基づく、ＳＯＩ基板を用いたＭＯＳトランジスタが完成する。

【図面の簡単な説明】

【図１】本発明に基づく複合構造体の基本構造を示す断面図。

【図２】本発明の製造方法で使用する活性酸素アニール装置の一例を示す断面図。

【図３】本発明の製造方法で使用する活性酸素アニール装置の他の一例を示す断面図。

【図４】本発明の製造方法で使用する活性酸素アニール装置の他の一例を示す断面図。

【図５】本発明の電子素子の一例として不揮発性メモリセルの構造を示す断面図。

【図６】本発明の電子素子の一例としてＳＯＩ基板上にＭＯＳトランジスタを形成した構造を示す断面図。

【図７】結晶性酸化物誘電体薄膜のリーク電流特性を示す特性図。

【図８】従来の電子素子構造に基づく不揮発性メモリセルの一例の断面図。

【図９】従来の電子素子構造に基づくＭＯＳトランジスタの一例の断面図。

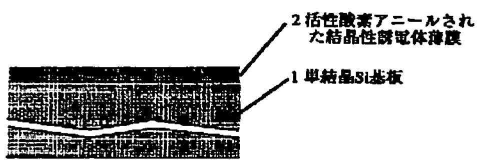
【符号の説明】

１…単結晶Ｓｉ基板　２…結晶性酸化物誘電体膜
１１…反応器　１２…真空ポンプ
１３…アニール前のＹＳＺ／Ｓｉ複合構造体
１４…サセプタ　１５…酸素ボンベ
１６…整圧器　１７…質量流量計
１８…誘電体バリヤ放電エキシマランプ
１９…合成石英窓　２０…排気バルブ
２１…大気排出バルブ　２２…真空排気装置
３１…アニール前CeO_2／Ｓｉ複合構造体
３２…オゾン発生器　３３…低圧水銀ランプ
４１…反応器　４２…真空ポンプ
４３…アニール前$SrTiO_3$／Ｓｉ複合構造体
４４…サセプタ　４５…パワー電極
４６…ブロッキング容量　４７…整合器

４８…高周波電源　４９…酸素ボンベ
５０…整圧器　５１…質量流量調節器
５２…排気バルブ　５３…圧力制御バルブ
６１…Ｓｉ基板　６２…フィールド酸化膜
６３…モート領域　６４…単結晶誘電体薄膜
６５…強誘電体膜　６６…ゲート電極
６７…ソース電極　６８…ドレイン電極
７１…Ｓｉ基板　７２…単結晶誘電体薄膜
７３…単結晶Ｓｉ膜　７４…フィールド酸化膜
７５…モート領域　７６…ポリシリコンゲート電極
７７…ゲート酸化膜　７８…ソース電極
７９…ドレイン電極

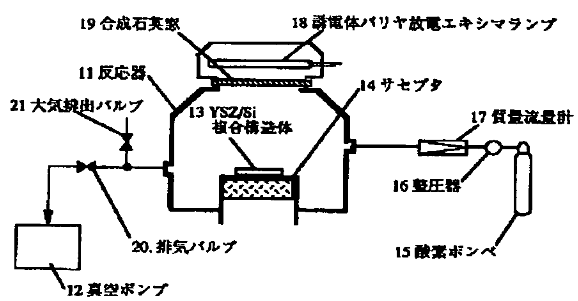
【図１】

（図１）



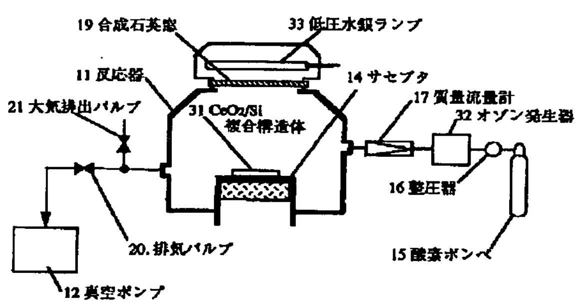
【図２】

（図２）



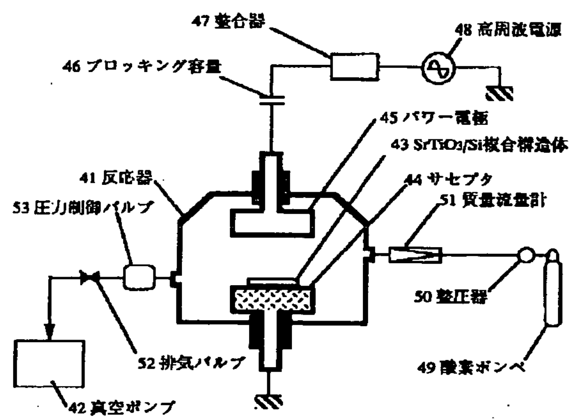
【図３】

（図３）



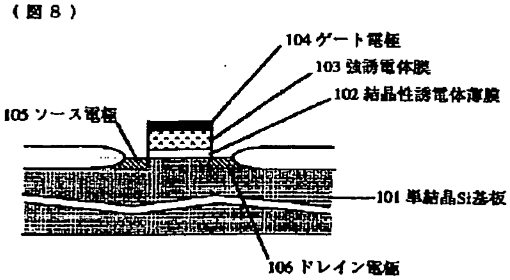
【図４】

（図４）



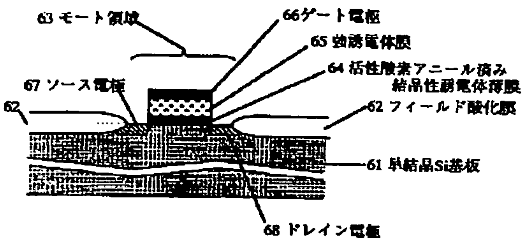
【図８】

（図８）



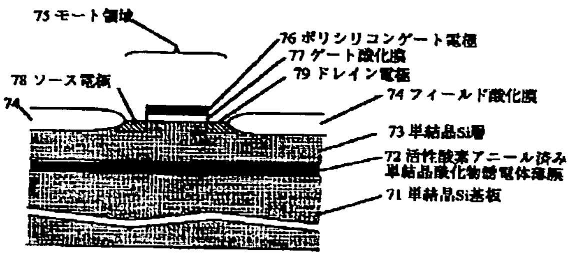
【図５】

（図５）



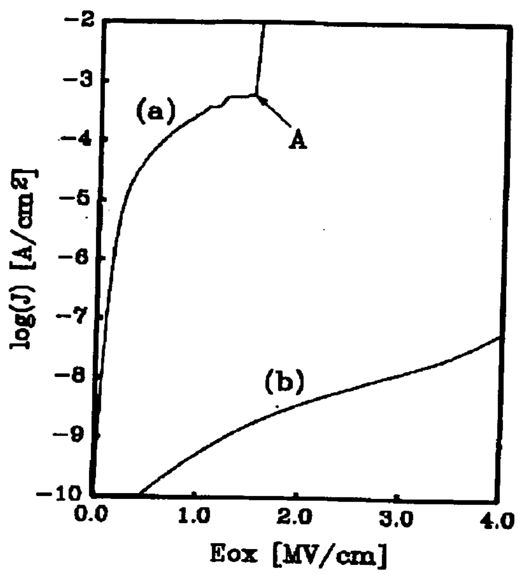
【図６】

（図６）



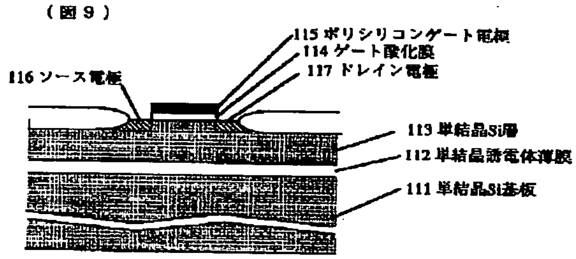
【図７】

（図７）



【図９】

（図９）



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(51) Int. Cl. 6	識別記号	F I	
H01L　21/8247		H01L　41/08	D
29/788			
29/792			
41/08			
49/00			

CLAIMS

[Claim(s)]
[Claim 1] The composite-construction object of the crystalline oxide dielectric thin film and single-crystal-silicon base which are characterized by the aforementioned crystalline oxide dielectric thin film being a thin film by which it was heat-treated in active oxygen atmosphere after growth in the composite-construction object which grew up the crystalline oxide dielectric thin film into the single-crystal-silicon semiconductor base.
[Claim 2] The electronic device to which the aforementioned composite-construction object is characterized by being the thin film by which it was heat-treated once [at least] in active oxygen atmosphere by the time it completed electronic device structure after the formation in the electronic device which includes the composite-construction object into which the crystalline oxide dielectric thin film was grown up in a single-crystal-silicon semiconductor base.
[Claim 3] The composite-construction object according to claim 1 with which the aforementioned crystalline oxide dielectric thin film is characterized by being the single crystal film which carried out hetero-epitaxial growth at the aforementioned single-crystal-silicon base, or an electronic device according to claim 2.
[Claim 4] A composite-construction object or an electronic device given in any of the claim 1 characterized by the bird clapper, or a claim 3 they are from the multilayer in which the aforementioned crystalline oxide dielectric thin film was formed of the laminating of two or more material.
[Claim 5] A composite-construction object or an electronic device given in any of the claim 1 characterized by being the monolayer or cascade screen from which the aforementioned crystalline oxide dielectric thin film was constituted by one or more material chosen from a stabilized zirconia, the cerium oxide, the strontium titanate, the magnesium oxide, and the yttrium oxide, or a claim 4 they are.
[Claim 6] The above-mentioned electronic device carries out the laminating of a crystalline oxide dielectric thin film (I), a ferroelectric thin film (F), and the metal-electrode film (M) to a part of single-crystal-silicon semiconductor base (S) at order. It is the MFIS transistor of the agenesis section of this cascade screen which prepared the source electrode and the drain electrode in part at least. An electronic device given in any of the claim 2 characterized by this crystalline oxide thin film being a thin film by which it was heat-treated once [at least] in active oxygen atmosphere after growth or ferroelectric thin film growth, or a claim 5 they are.
[Claim 7] The above-mentioned electronic device is an electronic device given in any of the claim 2 characterized by being the SOI substrate which grew epitaxially one or more crystalline oxide dielectric thin films (I) and single-crystal-silicon films on the single-crystal-silicon semiconductor base (S), and this crystalline oxide thin film being a thin film by which it was heat-treated once [at least] in active oxygen atmosphere after the growth, or a claim 5 they are.
[Claim 8] How to heat-treat under the UV irradiation in which heat treatment in the aforementioned active oxygen atmosphere contains the wavelength of less than 190nm while supplying oxygen, The method of heat-treating, while supplying ozone, the method of heat-treating under oxygen plasma, A composite-construction object given in any of the claim 1 characterized by being attained by the method

of overlapping when it differs, and performing the method of any one **, the method of performing simultaneously combining two or more methods, or two methods or more, or a claim 7 they are, or the manufacture method of an electronic device.
[Claim 9] A composite-construction object given in any of the claim 1 characterized by carrying out heat treatment in the aforementioned active oxygen atmosphere immediately after crystalline oxide dielectric thin film formation, or a claim 8 they are, or the manufacture method of an electronic device.
[Claim 10] The manufacture method of an electronic device given in any of the claim 2 characterized by being given after heat treatment in the aforementioned active oxygen atmosphere forms a crystalline oxide dielectric thin film and forms at least one of a conductive oxide or an oxide-semiconductor film, an oxides-superconductors film, and the oxide ferroelectric films on this crystalline oxide dielectric thin film, or a claim 8 they are.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture method of these structures or an electronic device at the composite-construction object of the very few crystalline oxide dielectric thin film of a leakage current, and a single-crystal-silicon (Si) substrate, the structure of the electronic device using this, and a row. In addition, the crystalline dielectric thin film said here shall mean the dielectric thin film which carried out priority orientation in the single crystal or the specific direction.
[0002]
[Description of the Prior Art] Generally the single crystal film has the feature that many physical properties flat in crystal structure and peculiar to the material, such as eye a uniform hatchet, conductivity, a dielectric, insulation, a ferroelectricity, superconductivity nature, a semiconductor property, light-transmission nature, optical magnetic properties, and crystal periodicity, appear keenly strongly, compared with the amorphous film or the polycrystal film. Therefore, it is useful in various industrial fields, and the realization is desired strongly. In recent years, these single crystal film is loaded into Si semiconductor device or an integrated circuit, and the attempt which is going to realize the high integrated circuit and high smart device of the added value which cannot be attained only with the conventional Si system material is performed actively, and is come and required. Basic structure indispensable when such a new Si semiconductor device is constituted is the composite-construction object (the following information-separator structure and abbreviated name) of a crystalline dielectric thin film (I) and a single crystal Si (S).
[0003] When an example is given, there is a MFIS type nonvolatile random access memory cell as shown in the typical structure section view of drawing 8 . This cell replaces O portion of an MOS transistor which consists of a (Metal M)-silicon-oxide (O)-semiconductor (S) by the single crystal ferroelectric film (F) which has electrically the spontaneous polarization which can be reversed, and the single crystal dielectric film (I).
[0004] In drawing 8 , it is the single crystal oxide dielectric film (I) by which 101 was carried out at the single crystal Si substrate of a p type field (100), and hetero-epitaxial growth of 102 was carried out on the Si substrate 101, for example, (100) is the YSZ film of a field. 103 is the ferroelectric film by which hetero-epitaxial growth was carried out on the single crystal oxide dielectric film 102, for example, (001) is $PbTiO_3$ film of a field. 104 is the gate electrode formed on the ferroelectric film 103, for example, is Pt electrode. 105 and 106 are n type source electrodes and drain electrodes, they carry out the ion implantation of P (Lynn) or the As (arsenic), respectively, make it activated by thermal diffusion, and are formed.
[0005] By this memory, information is recorded by impressing a positive or negative pulse voltage between gate (electrode G)-Si substrates (Sub), carrying out reversal fixation of the spontaneous-polarization vector of a ferroelectric film, and making a transistor into a flow or non-switch-on.
[0006] Moreover, as the above-mentioned ferroelectric layer, $PbTiO_3$ (lead titanate) film formed by the

chemical vapor growth (CVD), the magnetron sputtering method, etc., Pb(Zrx, Ti 1-x) O3 (zircon lead titanate) film, 3OBi4Ti12 (titanic-acid bismuth) film, etc. are examined (all are polarization shaft orientation single crystal films).

[0007] Moreover, as the above-mentioned single crystal dielectric layer, CeO2 (cerium oxide) film formed by the electron-beam-evaporation method or CVD, a YSZ (ITTORIYA stabilization JIRUKONIYA) film, SrTiO3 (strontium titanate) film, etc. are examined. These single crystal dielectric films are bearing a role of a buffer coat which prevents that function as a template layer for forming a single crystal ferroelectric film, and also Si substrate carries out counter diffusion to a ferroelectric.

[0008] Moreover, MFMIS structure is also proposed by the nonvolatile random access memory cell besides the above-mentioned MFIS structure. Single crystal F layer and M layers inserted between I layers of single crystals are here, the electric conduction films, for example, Pt film etc., of a single crystal etc. information-separator structure is used for the lower part of MFM structure also in this case.

[0009] Next, the MOS transistor of the SOI structure shown in the typical structure section view of drawing 9 is also the important application of information-separator structure. The MOS transistor of this structure has the feature which should be mentioned especially that it can escape from a very detrimental latch up completely on operation.

[0010] In drawing 9 , they are single crystal dielectric films, such as CeO2 by which hetero-epitaxial growth was carried out by 111 touching Si substrate of a field (100) and 112 touching this Si substrate 111, YSZ, and SrTiO3. This Si substrate 111 and the single crystal dielectric film 112 have constituted information-separator structure. The single crystal Si layer of the p type field (100) where hetero-epitaxial growth of 113 was carried out by CVD on the single crystal dielectric film 112, the SiO2 gate oxide film in which 114 was formed by thermal oxidation of the single crystal Si layer 113, and 115 are the gate electrodes of contest polysilicon formed by CVD and dry etching on the gate oxide film 114. 116 and 117 are the source electrodes and drain electrodes of N type, they carry out the ion implantation of P (Lynn) or the As (arsenic), respectively, make it activated by thermal diffusion, and are formed.

[0011] Moreover, the oxide high-temperature superconductivity thin film wiring tried aiming at high speed processing of an integrated circuit also forms quality single crystal superconductor film (for example, YBa2Cu 3O7) wiring on information-separator structure. As I layers, YSZ and the single crystal cascade screen of Y2O3 are used, for example.

[0012] Thus, it is understood that information-separator structure is the important basic structure for realizing various devices containing the functional thin film (a ferroelectric film, a semiconductor film, an electric conduction film, a superconductivity film, dielectric film) of a single crystal on a single crystal Si substrate. However, in the present condition, the problem that a low and (3) passage-of-time destructive (TDDB) life have short (2) disruptive strengths with large (1) leakage current is in I layers of single crystal oxide dielectric thin films, and it has been a serious obstacle at realization of the above highly efficient devices.

[0013] The above-mentioned problem is explained in detail based on actual data. Drawing 7 is the leakage-current property view of a crystalline oxide dielectric thin film. It is that a characteristic curve (a) indicates the example of a property of the conventional single crystal YSZ film to be in drawing 7 . On the YSZ film of the field (100) which grew epitaxially Si substrate of an N type single crystal (100) side Leakage-current density J [A/cm2] which impressed and measured positive voltage to the gate electrode of the MIS capacity which formed and produced aluminum electrode (gate) of a diameter 200 [mum] is shown as a function of field strength Eox [V/cm]. In addition, in order to remove an absorption current component, measurement of current is performed, after carrying out voltage impression and time passes enough. Moreover, thickness is 40 [nm] and the forming-membranes method is an electron-beam-evaporation method here. The forming-membranes methods (vacuum evaporationo conditions etc.) are later mentioned in the example of this invention in the cleaning-method row of a substrate.

[0014] The leakage current of the single crystal YSZ film of the conventional example is in a very high level so that the characteristic curve (a) of drawing 7 may be seen and may be known. Considering practical use, I want to suppress leakage-current density below to J= 1 [nA/cm2] at the time of field strength Eox=1[MV/cm]. However, in the above-mentioned conventional example, this and the value

which was greatly different widely are indicated to be the bases of J= 100 [muA/cm2]. Moreover, the current jump of A points in the characteristic curve (a) of drawing 7 shows that the YSZ film is carrying out dielectric breakdown on this voltage (Eox**1.5[MV/cm]). In order to apply to the above-mentioned MFIS nonvolatile memory cell etc., it is the value which cannot be said that this insulating disruptive strength is enough.
[0015] It is indispensable conditions that there is long-term dielectric-breakdown (TDDB) resistance over power supply stress in I more layers. This resistance measures and evaluates the amount Qbd of net charge [C/cm2] which passed the film by the time it generally gave and carried out dielectric breakdown of the constant-current stress to the dielectric film. The typical TDDB life when giving the constant-current stress of J= 0.1 [mA/cm2] to the above-mentioned single crystal YSZ film was Qbd=1.2 [mC/cm2], respectively. This value is a low comparable, if it compares with typical value Qbd-10 [C/cm2] of thermal oxidation SiO2 film used as gate oxide films, such as an MOS transistor. In order for power supply stress to apply a YSZ film to a comparatively strong MFIS nonvolatile memory cell etc., the TDDB life of the base of at least 0.1 [C/cm2] is required.
[0016] Such a problem of I layers in information-separator structure is not having restricted to the single crystal YSZ film formed by the electron-beam-evaporation method, but is a problem by which the YSZ film produced by other single crystal oxide dielectric-materials film and other forming-membranes methods is also observed in common.
[0017]
[Problem(s) to be Solved by the Invention] It is made in order that this invention may solve the trouble of the crystalline dielectric film (I layers) of the device which used such the conventional information-separator structure and this, and there are few leakage currents, dielectric-breakdown pressure-proofing is high, and the with-time dielectric-breakdown life aims at realizing a composite-construction object, the electronic devices using it, and those manufacture methods with information-separator structure, i.e., a crystalline oxide dielectric thin film, of having a crystalline, sufficiently long oxide dielectric layer, and a single-crystal-silicon base.
[0018]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, as information-separator composite-construction object, the electronic devices using this, and those manufacture methods were indicated to each patent claim, it constituted in this invention. That is, in invention according to claim 1, I layers presupposed that it is the crystalline oxide dielectric thin film which heat-treated in active oxygen atmosphere after growth in information-separator composite-construction object which grew up the crystalline oxide dielectric thin film into the single-crystal-silicon semiconductor base.
[0019] In the electronic device built on this in the claim 2 including information-separator composite-construction object, I layers presupposed similarly that it is the crystalline oxide dielectric thin film by which it was heat-treated in active oxygen atmosphere by the time it completed the electronic device after growth (active oxygen annealing is called below).
[0020] Claims 3-5 show the concrete mode of a claim 1 or a claim 2. That is, in a claim 3, it constitutes from a single crystal film which made the single-crystal-silicon base carry out hetero-epitaxial growth of the crystalline oxide dielectric thin film. Moreover, in a claim 4, the multilayer formed of the laminating of two or more oxide dielectric films constitutes the aforementioned crystalline oxide dielectric thin film. Moreover, it is supposed that it is the monolayer or laminating bipolar membrane as which the crystalline oxide dielectric thin film was chosen from a stabilized zirconia, the cerium oxide, the strontium titanate, the magnesium oxide, and the yttrium oxide in the claim 5.
[0021] Moreover, a claim 6 and a claim 7 show the concrete mode of an electronic device, and a claim 6 shows the case where the electronic device of a claim 7 is a SOI (Silicon On Insulater) substrate, when an electronic device is a MFIS transistor (MFIS type nonvolatile random access memory cell).
[0022] A claim 8 is a composite-construction object given in the aforementioned claim, or the manufacture method of an electronic device, and is in a manufacturing process. furthermore, active oxygen annealing of a crystalline oxide dielectric thin film How to heat-treat under the UV irradiation

which contains the wavelength of less than 190nm while supplying oxygen, The method of heat-treating, while supplying ozone, the method of heat-treating under oxygen plasma, The method of any one * , or the method of performing simultaneously combining two or more methods (for example, it heat-treats, supplying ozone under UV irradiation), Or it is attained by the method (the following method is performed after performing one method) of overlapping when it differs, and performing two or more methods. In addition, the range which has the capacity which decomposes oxygen and is made into active oxygen is meant in the wavelength of less than 190nm of the above-mentioned ultraviolet rays.

[0023] Moreover, a claim 9 is one mode of the manufacture method, and heat treatment in active oxygen atmosphere is carried out immediately after crystalline oxide dielectric thin film formation. Moreover, a claim 10 is one mode of the manufacture method of the aforementioned electronic device, and after heat treatment in active oxygen atmosphere forms a crystalline oxide dielectric thin film and forms at least one of a conductive oxide or an oxide-semiconductor film, an oxides-superconductors film, and the oxide ferroelectric films on this crystalline oxide dielectric thin film, it is given.

[0024] Hereafter, an operation is explained. First, the mechanism of the leakage current of the crystalline oxide thin film formed on the single crystal Si substrate is explained. According to the place which this invention person studied wholeheartedly and was clarified, the metal Si element of the oxygen vacancy inside the crystal grain of (1) oxide, the metallic element void inside (2) crystal grain, the energy level of (3) grain-boundary side, and (4) crystal-grain gap etc. is one of the causes of the leakage current of a crystalline oxide thin film, and a different (separation is impossible) leakage current based on each cause flows. The above-mentioned cause (1) and (2) are the so-called point defects from which the atom which should be in the lattice point of a crystal escapes probable. If a metallic element falls out, it will escape also from the oxygen atom combined with this in many cases together, and it will serve as a metal-oxygen void. An electron can move now easily between level and these point defects will cause the so-called hopping conduction, if electronic level is formed in the forbidden band of an oxide and this density becomes more than fixed. An amorphous film is also often observed and such a point defect causes a leakage current too.

[0025] The above-mentioned cause (1) and (2) are the causes peculiar to a crystalline oxide film about the leakage current to which a cause (3) and (4) flow a grain-boundary side to having been the cause of the leakage current which flows the inside of a grain boundary. Although an impression with strange "grain boundary" may be received in the crystalline oxide thin film which is growing epitaxially to the single crystal Si here, when this makes a single crystal Si carry out hetero-epitaxial growth of the dissimilar material from which a lattice constant is delicately different, in order to open the stacking-fault stress of a hetero side, it is the grain boundary produced inevitably, and the grain-boundary side is perpendicularly prolonged in the growth side. In this grain-boundary side, a crystal period is interrupted and many things which have not carried out a chemical bond exist in the atom which exists in a grain-boundary side. The above-mentioned cause (3) is the electronic level formed in the interior of a crystalline oxide forbidden band as a result in which these uncombined atoms exist. If electronic level becomes high concentration, a band will be formed and a leakage current will be increased. A cause (4) is the metal Si atom which invaded from Si substrate at the time of membrane formation of a crystalline oxide thin film, and segregated to the grain boundary. Since there is an opening about a 1 - number atomic layer in the grain boundary, the trap of the Si which has invaded from the substrate at the time of growth under reduced pressure (under hypoxia concentration) is carried out to a grain-boundary gap with a metal state (or low valence state). Naturally Si segregated to the grain boundary becomes the electric conduction path of a leakage current.

[0026] or this invention solves the conventional problem containing a leakage current how in the place which finished explaining the mechanism of generating of a leakage current (operation) -- ******** -- it explains According to this invention person's latest research result, it is thought that reduction of the leakage current by this invention takes place based on the following mechanisms. At active oxygen annealing of this invention, active oxygen, such as reactant high O (1D), and O2 (1deltag), O (3P), heat-treats comparatively a crystalline oxide thin film / single crystal Si structure at low temperature by the

atmosphere abundantly generated in the gaseous phase. At this time, active oxygen is diffused the inner direction toward Si substrate. A part of active oxygen encounters the oxygen vacancy of a cause (1), it extinguishes a vacancy (restoration), and is stabilized. Moreover, toward a grain boundary, a part of other active oxygen is diffused along with a grain boundary, and it oxidizes, sets to SiO2 the metal-like silicon which is carrying out the segregation to the grain boundary, and fills the grain-boundary gap section in SiO2 network. The metal Si of a cause (4) is removed by this. In addition, the above-mentioned heat treatment temperature is made into the range from ordinary temperature to about about 500 degrees C, and its about 200-500 degrees C are especially desirable. The reason is because active oxygen changes to usual oxygen at the elevated temperature of 500 degrees C or more and annealing time becomes long below 200 degrees C.

[0027] Furthermore, the uncombined hand atom M which existed in the grain boundary side is process in which SiO2 network is formed in a grain-boundary gap, accomplishes approaching Si and M-O-Si combination, and cancels the uncombined hand. A cause (3) is canceled by this. The remaining active oxygen is diffused to a single crystal Si substrate, and grows up a very thin SiO2 </SUB> film into a crystalline oxide thin film / Si interface. Although growth of SiO2 is generally accompanied by expansion of volume, since it is difficult to overcome compressive stress like the usual thermal oxidation, and to grow up, by active oxygen annealing, some Si elements are emitted into an oxide film, and oxidization by the interface advances at active oxygen annealing whose heat treatment temperature is low temperature, pressing down expansion of volume. Si atom emitted here encounters a metal-oxygen void in the process which carries out an out diffusion, and is captured in a metal atom position. On the other hand, at this time, from the gaseous phase, active oxygen is spread the inner direction, it enters in the middle of two or more metals of an oxide and Si atom which it is possible to encounter Si atom captured by the void, and approach a void, and M-O-Si combination is completed. In this way, the metal-oxygen void of a cause (2) is filled up by the Si-Ox (x=4-5) atomic group, and disappears. In addition, a large majority of Si atoms which were not captured by the void deposit on the front face of an oxide thin film. Since this sludge checks epitaxial growth of other thin films to a crystalline oxide thin film top, in this invention, it is removed by the fluoric acid solution etc. before growth.

[0028] In this way, according to the method, above-mentioned cause [of a leakage current] (1) - (4) is altogether removable in the structure row of this invention. Consequently, this invention can reduce the leakage current of a crystalline oxide thin film on the level of several figures compared with the conventional example so that it may mention later in the example.

[0029] An improvement of the amount Qbd of net charge which shows the insulating disruptive strength BEox and TDDB life by this invention below is described. It is hard to say that dielectric breakdown of crystalline oxide thin films, such as CeO2 made into the object of this invention and YSZ, and the mechanism of fatigue are in a research stage, and are fully solved. However, between field strength Eox, the amount Qbd of net charge, and leakage-current J, it is admitted widely that there is strong positive correlation. This has suggested that the factor and the cause of a leakage current of determining Eox and Qbd are common. Since it can remove the cause of the leakage current of a crystalline oxide as mentioned above, this invention can remove this, dielectric breakdown concerned deeply, and the factor of fatigue, as a result, compared with the conventional example, is high in the insulating disruptive strength BEox, and can enlarge the amount Qbd of net charge.

[0030]

[Effect of the Invention] As explained above, in this invention, it writes in the composite-construction object of a crystalline oxide dielectric thin film and a single crystal Si substrate as the film which gave active oxygen annealing after growing up this crystalline dielectric thin film, and the effect that (1) leakage-current property in a crystalline dielectric film, (2) insulation disruptive strength, and (3) with-time dielectric-breakdown (TDDB) resistance are improvable is acquired.

[0031] Moreover, in this invention, the effect that the destruction and the malfunction of an electronic device which originated in the poor property of above-mentioned (1) - (3), and had been produced are cancelable is acquired by applying the composite-construction object by the above-mentioned this invention to an electronic device including the composite-construction object of a crystalline oxide

dielectric film and a single crystal Si substrate.
[0032]
[Embodiments of the Invention] The manufacture method of of the electronic device which includes the composite-construction object of the crystalline oxide dielectric thin film and single crystal Si substrate concerning this invention and this composite-construction object hereafter, and a composite-construction object and an electronic device is explained based on the gestalt and example of operation.
[0033] (Gestalt of operation) Drawing 1 is the cross section showing the gestalt of 1 operation of the composite-construction object of the crystalline oxide dielectric thin film based on this invention, and a single crystal Si substrate. The single crystal Si substrate in which it sets to drawing 1 and 1 has the predetermined crystal faces, such as (100), (111), and a field (110), and 2 are the crystalline oxide dielectric thin film by which hetero-epitaxial growth was carried out on the Si substrate 1 in chemical vapor growths, such as physical vapor growths, such as an electron-beam-evaporation method, the ion beam sputtering method, a molecular beam epitaxy method, and the laser ablation method, and CVD, or a single crystal oxide dielectric thin film. Although the zirconia film (for example, YSZ film) stabilized by Y2O3, Sm2O3, CaO, etc., a cerium-oxide (CeO2) film, a strontium-titanate (SrTiO3) film, a yttrium-oxide (Y2O3) film, a magnesium oxide (MgO), etc. are mentioned as a dielectric thin film applicable to this, if it is the oxide dielectric thin film by which is not limited to this and hetero-epitaxial growth is carried out at Si substrate, other thin films are sufficient. After the oxide dielectric thin film 2 grows up to be the Si substrate 1, a predetermined time and heat treatment are performed to it at the temperature of under 500 [**] from ordinary temperature in active oxygen atmosphere, such as the Si substrate 1O3, O (1P), O (1D) and O2 (1deltag), and O2~. In this way, the composite-construction object based on this invention is completed.
[0034] Below, the example of the manufacture method of this invention will also be collectively explained by showing the process which produces this, while showing the concrete example of the form of operation of the above-mentioned this invention composite-construction object.
[0035] (Example 1) The concrete example of the beginning of the composite-construction object based on this invention is an example which builds the composite-construction object which consists of a single crystal Si substrate 1 of a field (100), and a single crystal ITTORIYA stabilized-zirconia (YSZ) thin film 2 of the epitaxially grown field (100) using a high-vacuum electron-beam-evaporation method and UV/O2 active-oxygen annealing. UV means the ultraviolet rays as a generation means of active oxygen here, and O2 means the oxygen as a raw material of active oxygen.
[0036] First, the surface contamination and surface natural oxidation object of the single crystal Si substrate 1 of a field (100) are removed by RCA washing (traditional Si substrate cleaning method which consists of washing by the mixed liquor of aqueous ammonia and hydrogen peroxide solution, and washing by the mixed liquor of a hydrochloric acid and hydrogen peroxide solution), and rare fluoric acid washing (cleaning method which carries out a rinse and which is dried with pure water after being immersed in HF solution of concentration for several 10 seconds 5%).
[0037] The YSZ film which continues and contains Y2O3 [about 13 mol %] on the Si substrate 1 is formed by the high-vacuum electron-beam-evaporation method. A vacuum evaporationo machine is general-purpose high-vacuum type equipment marketed as the object for an experiment, or an object for mass production. The target of vacuum evaporationo is the YSZ tablet with a diameter [of 15mm], and a thickness of 7mm which carried out cutting about a single crystal YSZ (Y2O313-mol%) ingot.
[0038] If the procedure of membrane formation is explained, an evaporation source will be filled up with a YSZ tablet, the washed Si substrate 1 will be installed in the substrate electrode holder of a vacuum evaporationo tub, and the inside of a vacuum evaporationo tub will be exhausted promptly. The substrate electrode holder has the capacity to heat a substrate to the temperature from ordinary temperature to 1000 [**], separated the distance of 30 [cm] and has opposed the source of vacuum evaporationo. Exhaust air of vacuum evaporationo equipment is powerful, and an internal pressure can be decompressed below to 10~9 [Torr]. If the pressure of a vacuum evaporationo tub amounts to 10~6 [Torr], substrate temperature will be heated and it will be made predetermined membrane formation temperature. A high-speed electron beam is made bombardment [in the place where temperature was

stabilized at and the pressure in a vacuum evaporationo tub fell below in 10~9 [Torr] / a tablet], and a YSZ film is grown up into Si substrate by the growth rate of 0.2 [nm/min]. Growth is continued until it gathers a growth rate to 5 [nm/min] and becomes predetermined thickness, while introducing high grade dryness oxygen into a vacuum evaporationo tub from the exterior in the place where the thickness of YSZ became 3 [nm] in general and adjusting a pressure to 2x10~6 [Torr]. A growth rate controls and adjusts the emission current of hot cathode. (100) The typical membrane formation conditions from which the single crystal YSZ thin film of a field is obtained are as follows.

[0039]

------------------------------------ YSZ membrane formation conditions Membrane formation pressure
1x10~8 [Torr] (up to 3nm of thickness)
2x10~6 [Torr] (from 3nm of thickness to O2 introduction)
Membrane formation temperature 800 [**] (substrate temperature)
Target Y2O3:ZrO 2= 13:87 Substrate distance 30cm Electron beam acceleration voltage The output of a vacuum evaporationo power supply is cut in the place where 8kV ------------------- -----------------
thickness became a desired value, and membrane formation is finished. Then, a substrate is annealed putting a substrate on a vacuum evaporationo tub, and after substrate temperature becomes sufficiently low, a substrate is taken out from a vacuum evaporationo tub. Thus, the deposited YSZ film was a single crystal epitaxial film which has fluorite structure (cubic).

[0040] The composite-construction object of the YSZ thin film and single crystal Si which were explained above as a conventional example is completed at the process so far. However, with the composite-construction object based on this invention, an active oxygen annealing process is carried out after this. Although one of the active oxygen annealing and the example of UV/O2 annealing explain here, other below-mentioned active oxygen annealing is sufficient.

[0041] Drawing 2 is the typical important section cross section of the equipment used for annealing. In drawing 2 , the reactor with which, as for 11, water cooling of the side attachment wall is carried out, and 12 are the vacuum pumps for exhausting a reactor 11, and can maintain the pressure of a reactor 11 from an ordinary pressure before 10~6 [Torr]. 13 is a composite-construction object in front of annealing which grew up the single crystal YSZ thin film to be a single crystal Si substrate. 14 is a susceptor for supporting 13 and holding to predetermined temperature. The composite-construction object 13 is placed so that a YSZ film surface may be upwards suitable on a susceptor 14. 15 is the chemical cylinder filled up with oxygen O2 of 99.999% or more of purity. After O2 of a bomb is decompressed by ready **** 16 on the occasion of annealing by the pressure about 0.5 [kg/cm2], it is adjusted by the flow rate predetermined with the mass flow rate controller 17, and is led to a reactor 11. 18 is the dielectric barrier electric discharge excimer lamp with which xenon gas was enclosed, and can generate the ultraviolet radiation UV with the main powerful wavelength 172 [nm]. Incidence of the ultraviolet exciting line by which outgoing radiation was carried out is carried out to the reactor 11 interior through the synthetic quartz aperture 19 from the excimer lamp 18. The exhaust air bulb which opens and closes the exhaust pipe arrangement with which 20 connects a vacuum pump 12 to a reactor 11, and 21 are atmospheric-exhaust bulbs. In addition, the wavelength of the above-mentioned ultraviolet radiation is the value of the range which has the capacity which decomposes oxygen and is made into active oxygen, and needs to be less than 190nm generally.

[0042] The following procedures perform UV/O2 annealing. Opening of the exhaust air bulb 20 is carried out, and evacuation of the inside of a reactor 11 is immediately carried out at the same time it carries the composite-construction object 13 on the susceptor 14 currently heated by predetermined temperature and operates a vacuum pump 12. The exhaust air bulb 20 is embarrassed in the place where the internal pressure arrived at the base of 10~5 [Torr], a vacuum pump 12 is suspended, and high grade O2 gas is introduced into a reactor 11 with the mass flow rate about 1000 [cc/min]. In the place where the internal pressure of a reactor turned into an ordinary pressure (= atmospheric pressure), opening of the atmospheric-exhaust bulb 21 is carried out, and O2 surplus gas introduced henceforth is discharged out of a reactor 11 with a predetermined mass flow rate. A reactor 11 is maintainable in the pure oxygen atmosphere of atmospheric pressure by carrying out like this. Outgoing radiation of the ultraviolet

exciting line is continuously carried out to the reactor 11 interior from the excimer lamp 18. The ultraviolet radiation of the 172 [nm] wavelength which carried out incidence to the reactor 11 interior is strongly absorbed to O2 in a reactor 11, and the active oxygen which consists of O3, O (3P), O (1D), O2 (1deltag), etc. generates it as a result. In the place where the above preparation was completed, UV/O2 active-oxygen annealing is carried out predetermined time. Typical annealing conditions are shown below.

[0043]

------------------------------------ Active oxygen annealing (UV/O2) conditions Container pressure Atmospheric pressure Processing temperature 350 [**]

Excitation intensity (synthetic quartz glass position) 13 [mW/cm2] (172 [nm])

O2 flow rate 200 [cc/min]

Processing time 15 [min]

If ------------------ ----------------- annealing is completed, the outgoing radiation of the excimer lamp 18 and introduction of a high grade O2 will be stopped, and the composite-construction object 13 will be taken out immediately. In this way, UV/O2 annealing finishes and the composite-construction object of the crystalline oxide dielectric thin film of this invention and a single crystal Si substrate is completed.

[0044] In addition, the above-mentioned processing temperature (annealing temperature) is made into the range from ordinary temperature to about about 500 degrees C, and its about 200-500 degrees C are especially desirable. According to the experimental result, active oxygen changes to usual oxygen at the elevated temperature of 500 degrees C or more, and annealing time becomes long below 200 degrees C.

[0045] Next, it explains, making the effect of the example of this invention contrast with the survey data of the conventional example. The characteristic curve (b) of drawing 7 shows the leakage-current (current which flows on YSZ film) property which impressed and measured positive voltage in the MIS capacity which carried out the vacuum evaporationo of the aluminum gate electrode, and formed it on the YSZ film in the composite-construction object of the YSZ/Si substrate produced based on the above-mentioned example 1. In addition, a characteristic curve (a) is the leak property (previous statement) of the composite-construction object by the conventional example.

[0046] If (b) is compared with the characteristic curve (a) of drawing 7 , it turns out that the example of this invention is reducing the leakage current by 4 figures - 5 figures in general compared with the conventional example. If the property of Eox=1[MV/cm] is seen, in the example of this invention, the value below J= 1 [nA/cm2] is given to the conventional example being a current density J= 100 [muA/cm2] base.

[0047] Next, although it was BEox=1.5[MV/cm] in the conventional example according to measurement when its attention was paid to the insulating disruptive strength BEox, BEox=4.6[MV/cm] and improvement in 3 or more times were found in this invention example.

[0048] moreover, the TDDB life when giving constant-current stress 0.1 [mA/cm2] -- the conventional example -- amount Qbdof net charge = -- 1.2 [mC/cm2] -- it was (previous statement) -- receiving -- the example of this invention -- Qbd= -- it is the value of 850 [mC/cm2] and the improvement of about 3 figures was obtained

[0049] From the above result, it is understood that this invention is very effective in reduction of (1) leakage current of the crystalline oxide thin film in the composite-construction object of a crystalline oxide thin film / Si substrate, improvement in (2) insulation disruptive strength, and impudence of (3) TDDB life.

[0050] (Example 2) The 2nd concrete example of the composite-construction object based on this invention is an example which forms the composite-construction object which consists of a single crystal Si substrate of a field (100), and a single crystal cerium-oxide (CeO2) thin film 2 of the field (110) grown epitaxially using a high-vacuum electron-beam-evaporation method and UV/O3 active-oxygen annealing. "/O3" means the oxygen as a raw material containing 8% of ozone O3 here.

[0051] First, n type the surface contamination and surface natural oxidation object of a single crystal Si substrate of a field (100) are removed by RCA washing and rare fluoric acid washing. PITAKISHARU growth of the CeO2 thin film is continuously carried out by the high-vacuum electron-beam-evaporation

method on Si substrate. A vacuum evaporationo machine uses the same thing as the equipment used by the aforementioned YSZ growth. A vacuum evaporationo target is the tablet which fabricated and made CeO2 powder of 99.999% or more of purity with the hotpress the form of a diameter 15 [mm] and thickness 7 [mm]. An evaporation source is filled up with CeO2 tablet, Si substrate is installed in the substrate electrode holder of a vacuum evaporationo tub, and the inside of a vacuum evaporationo tub is exhausted. If the pressure of a vacuum evaporationo tub amounts to 10~6 [Torr], substrate temperature will be heated and it will be made predetermined membrane formation temperature. Temperature is stabilized, a high-speed electron beam is made bombardment [in the place where tub internal pressure fell below in 10~9 [Torr] / a tablet], and CeO2 film is grown up by the growth rate of 0.4 [nm/min]. Growth is continued until it gathers a growth rate to 1.55 [nm/min] and becomes predetermined thickness, while introducing high grade dryness oxygen into a vacuum evaporationo tub in the place where thickness became 5 [nm] in general and adjusting a pressure to 8x10~6 [Torr]. A growth rate controls and adjusts the emission current of hot cathode. The typical membrane formation conditions from which single crystal CeO2 thin film of the above-mentioned (110) field is obtained are as follows.
[0052]
----------------------------------- (110) CeO2 membrane-formation conditions of a field Membrane formation pressure Below 1x10~8 [Torr] (up to thickness 3 [nm])
8x10~6 [Torr] (from thickness 3 [nm] to O2 introduction)
Growth temperature 800 [**] (substrate temperature)
Target 99.999% CeO2 of purity tablet Substrate distance 30cm Electron beam acceleration voltage The output of a vacuum evaporationo power supply is cut in the place which became the thickness of a 8kV -
------------------ ----------------- request, and membrane formation is finished. Thus, CeO2 deposited film was a single crystal epitaxial film of a field which has fluorite structure (cubic) (110). It is also possible to obtain single crystal CeO2 film of the field where the directions of orientation incidentally differ on Si substrate of the same (100) field (111). In this case, growth temperature is set to 600 [**] in the above-mentioned growth conditions. The conventional example is completed in this stage. With the composite-construction object based on this invention, an active oxygen annealing "UV/O3 annealing" process is carried out after this.
[0053] Drawing 3 is the typical important section cross section of the equipment used for annealing. Since the function and composition of the part which attached the same number as drawing 2 are the same as drawing 2 , redundancy is avoided and explanation is omitted. In drawing 3 , 31 is CeO2 / Si composite-construction object on the way of a process. The silent-discharge type ozonator 32 is installed between ready **** 16 and the mass flowmeter 17. This ozonator 32 can generate O3 [eight mol %] for oxygen in a raw material. 33 is a low-pressure mercury lamp and can generate ultraviolet radiation with wavelength 185 [nm] and the bright line strong against 254 [nm]. Incidence of the ultraviolet exciting line by which outgoing radiation was carried out is carried out to the reactor 11 interior through the synthetic quartz aperture 19 from a low-pressure mercury lamp 33.
[0054] The procedure of UV/O3 annealing is almost the same as the UV/O2 above-mentioned annealing. That is, the structure 31 is carried on the susceptor 14 of predetermined temperature, and evacuation of the inside of a reactor 11 is carried out immediately. The exhaust air bulb 20 is embarrassed in the place where the pressure of the reactor 11 interior arrived at the base of 10~5 [Torr], a vacuum pump 12 is suspended, and high grade O2 gas is introduced into a reactor 11 with the mass flow rate about 1000 [cc/min]. High grade O2 gas which an ozonator 32 is operated and contains 8% of O3 in the place where the internal pressure of a reactor 11 turned into an ordinary pressure (= atmospheric pressure) at the same time it carries out opening of the atmospheric-exhaust bulb 21 is introduced into a reactor 11. Between is not kept but outgoing radiation of the ultraviolet exciting line is carried out to the reactor 11 interior from a low-pressure mercury lamp 33. The ultraviolet radiation of 254 [nm] which carried out incidence to the reactor 11 interior photodissociates O3 in a vessel, and the active oxygen which consists of O (1D), O2 (1deltag), O (3P), etc. besides O3 generates it as a result. In this way, UV/O3 active-oxygen annealing is carried out predetermined time. The typical annealing conditions are as follows.

[0055]
------------------------------------ Active oxygen annealing (UV/O3) conditions Container pressure Atmospheric pressure Processing temperature 400 [**]
Excitation intensity (synthetic quartz glass position) 20 [mW/cm2] (254 [nm])
O2 flow rate 200 [cc/min]
Processing time 60 [min]
If ------------------ ---------------- annealing is completed, the outgoing radiation of a low-pressure mercury lamp 33, the operation of an ozonator 32, and introduction of a high grade O2 will be stopped, and a composite-construction object will be taken out immediately. In this way, the composite-construction object of the crystalline oxide dielectric thin film and single crystal Si substrate by this invention is completed.
[0056] Next, the effect of this example 2 is explained. The following table 1 is a table which compared the TDDB life (the amount Qbd of net charge) when giving leakage-current JL in the field strength 1 [MV/cm] of CeO2 thin film (20 [nm]) of the CeO2/Si composite-construction object based on the conventional example, the insulating disruptive strength BEox, and a constant current 0.1 [mA/cm2] to this example 2 row.
[0057]
[Table 1]
（表１）

ＣｅＯ$_2$／Ｓｉ複合構造体の電気特性の比較

	リーク電流ＪＬ ［ｎＡ／ｃｍ^2］	絶縁破壊強度ＢＥox ［ＭＶ／ｃｍ］	総電荷量Ｑｂｄ ［ｍＣ／ｃｍ^2］
実施例	０．４５	５．１	１８００
従来例	３５００	１．４	１２．４

[0058] The electrical property of the above-mentioned table 1 impressed and measured positive voltage in MIS capacity (aluminum gate) like the aforementioned example 1. As [from Table 1] the Ming kana, the example 2 of this invention reduces a leakage current JL by 4 figures in general compared with the conventional example, and is raising the insulating disruptive strength BEox 3.5 times. Furthermore, the amount Qbd of net charge corresponding to a TDDB life was put on two 1 C/cm, and it succeeded in raising a TDDB life by 2 figures conventionally. That it is effective for the leakage current of the crystalline oxide thin film in the composite-construction object of a crystalline oxide thin film / Si substrate or an improvement of an insulating disruptive strength and a TDDB life has the clear example 2 of the above result to this invention.
[0059] In addition, in the above-mentioned active oxygen annealing, it is also possible to transpose to annealing which does not use UV, i.e., O3 annealing. Since O3 annealing also produces active oxygen, it is effective. Although the composition of a thermal treatment equipment becomes easy from UV/O3, compared with the time of heat treatment time using UV, it is extended a double-precision grade. Moreover, other active oxygen annealing methods of the above-mentioned example or the below-mentioned example can be used.
[0060] (Example 3) The 3rd concrete example of the composite-construction object based on this invention is an example which forms the composite-construction object which consists of a single crystal Si substrate 1 of a field (100), and a single crystal strontium-titanate (SrTiO3) thin film 2 of a

field (001) by the laser ablation vacuum deposition and plasma/O2 annealing.
[0061] After removing n type the surface contamination and surface natural oxidation object of a single crystal Si substrate of a field (100) by RCA washing and rare fluoric acid washing, SrTiO3 thin film is grown up in a high-vacuum laser ablation vacuum deposition on Si substrate. A vacuum evaporationo machine is a general aviation equipped with two switchable sources of vacuum evaporationo in the vacuum. Each source of vacuum evaporationo is filled up with the SrO tablet and SrTiO3 tablet which operated the powder of 99.999% or more of purity orthopedically in the shape of a disk (10phi, 10t) with the hotpress.
[0062] If the procedure of growth is explained, the Si substrate 1 immediately after the aforementioned washing will be installed in the substrate electrode holder in a vacuum evaporationo tub, and the inside of a vacuum evaporationo tub will be exhausted. This electrode holder has the capacity to heat a substrate to the temperature from ordinary temperature to 800 [**], and has opposed on both sides of the distance of about 5 [cm] from the tablet. Exhaust air of vacuum evaporationo equipment is powerful, and an internal pressure can lower back pressure to below 10~9 [Torr]. A substrate electrode holder is heated in the place where the pressure of a vacuum evaporationo tub amounted to 10~8 [Torr], and it is made predetermined growth temperature. The preparations which use the 1st evaporation source with which SrO will be filled up by the time temperature is stabilized are made.
[0063] Turn on the output of a laser light source in the place where the pressure in a vacuum evaporationo tub fell below in 10~8 [Torr], a high-density laser beam is made bombardment [a tablet], and growth of a very thin SrO buffer film is started. The laser of this example is a KrF (wavelength [of 248nm], 20ns of pulse width) excimer laser. Repeat frequency was 10 [Hz] and the energy density was 1.0 [J/cm3]. The thickness of a SrO buffer film suspends the output of laser by ****** set to 6 [nm], and stops growth. While changing an evaporation source to the 2nd evaporation source in which SrTiO3 tablet is stored immediately, the temperature of a substrate electrode holder is changed into the predetermined temperature suitable for SrTiO3 growth. In the place by which temperature was stabilized, high grade oxygen is introduced from the exterior, a pressure is set to 5x10~5 [Torr], the output of laser is turned on again, and SrTiO3 film is grown up shortly. Dispatch of a laser light source is stopped in the place where thickness became a desired value, introduction of O2 is stopped, and a substrate is annealed. It is as follows when an example of the growth conditions from which SrTiO3 film of a single crystal (001) side is obtained is summarized.
[0064]
------------------------------------ Growth conditions of a SrO buffer film Growth pressure Below 1x10~8 [Torr] Growth temperature 800 [**] (substrate temperature)
Tablet-substrate distance 5 [cm]
Laser light source KrF excimer laser (energy 130mJ)
Excitation pulse 20ns of width of face, repeat frequency 10Hz------------------------------------ Growth conditions of SrTiO3 film Growth pressure 5x10~5 [Torr] (99.999% oxygen introduction)
Growth temperature 600 [**] (substrate temperature)
Other conditions take out a substrate from a vacuum evaporationo tub, after the same ------------------- ---
-------------- substrate temperature as upper SrO becomes sufficiently low. the SrO layer of 6 [nm] formed first disappears in process in which SrTiO3 next film is grown up (it is thought that it deteriorated on SrTiO3 film) -- it is -- the film formed in this way is single crystal SrTiO3 monolayer as a matter of fact
[0065] The conventional example is completion with the composition of this stage. With the composite-construction object based on this invention, active oxygen annealing is performed after this. Although the UV/O2 above-mentioned annealing and UV/O3 annealing are also possible, the example of "plasma/O2 annealing" is introduced here.
[0066] Drawing 4 is the typical important section cross section of the equipment used for plasma/O2 annealing. In drawing 4 , the reactor with which, as for 41, water cooling of the side attachment wall is carried out, and 42 are the vacuum pumps for exhausting a reactor 41, and can maintain the pressure of a reactor 41 from an ordinary pressure before 10~6 [Torr]. 43 is a composite-construction object in front

of annealing. 44 is the susceptor equipped with a heating means to support the composite-construction object 43 and to hold to predetermined temperature. This susceptor 44 is grounded electrically. The composite-construction object 43 is put on a susceptor 44 so that $SrTiO_3$ film surface may be upwards suitable. The power electrode 45 is placed so that a susceptor 44 may be opposed. The power electrode 45 is electrically connected to RF generator 48 (for example, frequency of 13.56MHz) besides a vessel through the blocking capacity 46 and the adjustment machine 47. 49 is the chemical cylinder filled up with oxygen O_2 of 99.999% or more of purity. After 49 chemical cylinderO_2 is decompressed by ready **** 50 by the pressure about 0.5 [kg/cm2], it is adjusted by the flow rate predetermined with the mass flow rate controller 51, and is led to a reactor 41. The exhaust air bulb which opens and closes the exhaust pipe arrangement with which 52 connects a vacuum pump 42 to a reactor 41, and 53 are pressure-control bulbs which control the pressure of a reactor uniformly.
[0067] The procedure of plasma/O_2 annealing is as follows. Opening of the exhaust air bulb 52 is carried out, and evacuation of the inside of a reactor 41 is immediately carried out at the same time it carries the composite-construction object 43 before processing on the susceptor 44 currently heated by predetermined temperature and operates a vacuum pump 42. While introducing high grade O_2 gas into a reactor 41 with a predetermined mass flow rate in the place where the pressure of the reactor 41 interior arrived at the base of 10~5 [Torr], the pressure-control bulb 53 is operated, and the internal pressure of a reactor 41 is adjusted to a predetermined value. After waiting until internal pressure and susceptor temperature are stabilized, turn on the output of RF generator 48, electric discharge is made to cause between a susceptor 44 and the power electrode 45, and annealing is started. If electric discharge takes place, the active oxygen which consists of O_3, O (3P), O (1D), O_2 (1deltag), etc. will occur. In the place where the above preparation was completed, UV/O_2 active-oxygen annealing is carried out predetermined time. Typical annealing conditions are shown below.
[0068]
----------------------------------- Active oxygen annealing (plasma/O_2) conditions Container pressure 3 [mTorr]
Processing temperature 400 [**]
Susceptor-power inter-electrode distance 30 [cm]
O_2 flow rate 1 [cc/min]
RF power 100 [W]
Processing time 20 [min]
Annealing will be ended if ------------------ ----------------- predetermined time passes. That is, a RF output is suspended, the operation of the pressure-control bulb 53 is stopped, the exhaust air bulb 52 is closed, a vacuum pump 42 is suspended, air is introduced into a reactor 41, air opening is carried out, and the composite-construction object 43 is taken out out of a vessel. Such is carried out and the composite-construction object of single crystal $SrTiO_3$ film and a single crystal Si substrate is completed.
[0069] Next, the effect of the example 3 of this invention is explained. The following table 2 is a table which measured the amount Qbd of net charge when giving leakage-current JL in the field strength 1 [MV/cm] of $SrTiO_3$ thin film (40nm), the insulating disruptive strength BEox, and a constant current 0.1 [mA/cm2] with the example 3 row in the $SrTiO_3$/Si composite-construction object based on the conventional example.
[0070]
[Table 2]

（表２）

ＳｒＴｉＯ$_3$／Ｓｉ複合構造体の電気特性の比較

	リーク電流ＪＬ ［ｎＡ／ｃｍ²］	絶縁破壊強度ＢＥox ［ＭＶ／ｃｍ］	総電荷量Ｑｂｄ ［ｍＣ／ｃｍ²］
実施例	０．０８９	４．９	１３５０
従来例	２２０	２．３	８．１

[0071] The electrical property of Table 2 impressed and measured positive voltage in MIS capacity (aluminum gate) like the aforementioned example. As shown in Table 2, in an example 3, compared with the conventional example, a leakage current JL is reduced 3-figure strength, and the insulating disruptive strength BEox is raised to double precision. Furthermore, the amount Qbd of net charge corresponding to a TDDB life was increased by 3 figures, and it succeeded in putting Qbd on the base of 1 [C/cm2]. It is shown that the above result is the technology which the example 3 of this invention can greatly contribute to the leakage current of a crystalline oxide thin film and the improvement of reliability in the composite-construction object of a crystalline oxide thin film / Si substrate.
[0072] the effect of improving the leakage current and reliability of a crystalline oxide thin film of such a composite-construction object is an effect of appearing equally also to other single crystal oxide thin films and stacking-tendency oxide thin films which are not limited to the YSZ film explained in the concrete example to here, CeO2 film, and SrTiO3 film, and were grown up into Si single crystal substrate, and the scope of this invention is wide However, the optimum conditions of active oxygen annealing differ according to the target composite-construction object.
[0073] Moreover, on account of explanation, although all were made into the monolayer, as for the composition of a crystalline oxide thin film, an improvement effect with the same said of the cascade screen of a film of a different kind is acquired. For example, the remarkable leak mitigation effect, an insulating disruptive strength, and a TDDB resistance improvement effect show up also with the CeO2/SrTiO3/Si composite-construction object which carried out the laminating of the CeO2 single-crystal film of a field (001), and the SrTiO3 single-crystal film of a field (001).
[0074] Next, the example which applied this invention to the electronic device is explained.
(Example 4) this example is an example which applied information-separator composite-construction object shown in aforementioned drawing 1 to the MFIS type nonvolatile memory cell.
[0075] Drawing 5 is the typical structure section view of a MFIS type nonvolatile random access memory cell. Although this cellular structure is the same as the conventional cellular structure apparently explained by aforementioned drawing 8 , the places whose crystalline oxide dielectric thin films I are films to which active oxygen annealing was given differ greatly. In drawing 5 , the place in which 61 is the single crystal Si substrate of a p type field (100) and the thick field oxide film by which 62 was alternatively formed on Si substrate, and this field oxide film 62 is not formed is the MORT field 63. The memory cell is formed in this MORT field 63. 64 is the single crystal oxide dielectric film by which hetero-epitaxial growth was carried out to the MORT field (I), for example, (100), the YSZ film of a field, and is the film to which active oxygen annealing was given by the time the element was completed. On the single crystal oxide dielectric film 64, the ferroelectric film 65, for example, (001), PbTiO3 film of a field, and the gate electrode 66, for example, Pt electrode, are. The ferroelectric film 65 is carrying out hetero-epitaxial growth on the crystalline oxide dielectric thin film 64. 67 and 68 are n type impurities, for example, the source electrode and drain electrode by which P and As are doped by

high concentration.
[0076] Next, if the main point of the manufacturing process of this element is explained briefly, after removing the contamination of the front face of the single crystal Si substrate of a p type field (100) by RCA washing first, the thermal oxidation film of 40 [nm] will be formed in the front face of Si substrate by the oxidizing [thermally] method, and Si3N4 film (it is written as a SiN film below) of 150 [nm] will be further formed by the LPCVD method on it. It continues, leaves the portion equivalent to the MORT field using phot lithography and the plasma etching method, and a SiN film (and thermal oxidation film) is removed. Next, after exfoliating and carrying out RCA washing of the resist again, the field oxide film of 400 [nm] is formed by the oxidizing [thermally] method (LOCOS oxidization). At this time, since an oxide film does not grow up to be the portion in which the SiN film is formed, the MORT field is also formed in it together with a field oxide film. Then, heat phosphoric acid removes a SiN film.
[0077] It continues and the YSZ film of a single crystal (001) side is grown up to be the MORT field. After removing the contamination and natural oxidation film of the MORT field by RCA washing and cleaning with diluted hydrofluoric acid, the YSZ film which contains Y2O3 [about 13 mol %] all over a substrate is grown up in a 20[nm] high truth atmospherics beam vacuum deposition. Since the example of the above-mentioned composite-construction object explained this membrane formation, explanation is not repeated here. After growth of a YSZ film finishes, a substrate is made immersed in the rare fluoric acid of concentration for about 10 seconds 1%, and by ultrapure water, a rinse is carried out and it dries.
[0078] In the place which washing by rare fluoric acid finished, the single crystal PbTiO3 of a field (001) is grown up using the MOCVD (organic-metal vapor growth) method. The raw materials to be used are the tetraethyl lead [Pb (C2H5)4], and tetraisopropoxy titanium [Ti (i-OC3H7)4] and dryness oxygen (O2). Front 2 persons are liquids in an ordinary temperature ordinary pressure, evaporate all with a carburetor and convey them to a reactor by dryness Ar carrier gas. Growth equipment uses not special equipment but a general aviation. The typical membrane formation conditions are as follows.
[0079]
------------------------------------ (001) MOCVD growth conditions of the single crystal PbTiO3 of a field
Growth pressure 6 [Torr]
Growth temperature 640 [**] (substrate temperature)
Field Charge Pb (C2H5)4, Ti (i-OC3H7)4, O2 Evaporation temperature -15 degrees C [Pb (C2H5)4] 25 degrees C [Ti (i-OC3H7)4]
A quantity of gas flow O2 100 cc/min Pb raw material carrier (Ar) 25 cc/min Ti raw material carrier (Ar) 22 cc/min Ar dilution 200cc/min------------------------------------ a degree -- active oxygen annealing, for example, UV/O3 annealing, -- predetermined time operation -- it carries out detailed explanation of UV/O3 annealing is already described -- it comes out and omits The leakage-current property of not only a YSZ film but the three or so PbTiO(s) dielectric film which grew previously, and an insulating disruptive strength and TDDB resistance are simultaneously improvable with this active oxygen annealing. In addition, even if it performs active oxygen annealing immediately after YSZ film formation, although it is good of course, an improvement of the electrical property of a ferroelectric film cannot be desired in this case.
[0080] If growth of a ferroelectric film is ended, next, complete membrane formation of the gate electrode material Pt, for example, platinum, will be performed. Membrane formation of Pt uses the general-purpose DC magnetron sputtering method. As an electrode material, Pt target more than 99.99% purity and thickness are 100 [nm] **. The typical sputtering membrane formation conditions of Pt are as follows.
[0081]
------------------------------------ DC MAKUNE TRON sputtering conditions of Pt Membrane formation pressure 3 [mTorr]
Membrane formation temperature 400 [**] (substrate temperature)
Field Charge 99.99%Pt target Spatter gas Ar Target-substrate distance 30 [cm]

DC power 150 [W]
------------------------------------ if membrane formation of Pt ends, Pt gate electrode will be formed using a photolithography and Ar sputter-etching technology The resist which etching of Pt ended is left as it is, and reactive ion etching of PbTiO3 film and a YSZ film is performed continuously. Etching gas is the mixed gas of CF4 and O2. If etching of a YSZ film is completed, a resist will be made to ash, it will remove and the dust on the front face of a substrate will be removed by ultrasonic cleaning using the organic solvent.

[0082] It continues and the ion implantation of the P is carried out all over a substrate. The portion except the gate electrode of the MORT field, i.e., the source, and a drain field are poured into Si substrate. Acceleration voltage is 100 [keV] and a dose is 5x1015 [an individual / cm2]. If an ion implantation is completed, activation of the source and the pouring impurity of a drain will be performed using rapid heat treatment (RTA) equipment. Heat treatment temperature is 1200 [**] and heat treatment time is 30 seconds. Thus, a MFIS type ferroelectric memory cell is completed.

[0083] (Example 5) Other examples of an electronic device are examples in which the MOS transistor was formed on the SOI substrate which used information-separator composite-construction object of the aforementioned this invention. Drawing 6 is the typical structure section view of the MOS transistor of SOI structure. The places whose crystalline oxide dielectric thin films pinched between Si epitaxial film and Si single crystal substrate are films to which active oxygen annealing was given although this structure is the same as the structure of the conventional example where it explained by drawing 9 , seemingly differ greatly.

[0084] In drawing 6 , it is the film to which active oxygen annealing was given by the time the single crystal Si substrate of the field (100) of n form where the impurity dope of 71 was carried out at high concentration, and 72 are the single crystal oxide dielectric films by which hetero-epitaxial growth was carried out on the Si substrate 71 (I), for example, (100), the YSZ film of a field, and the element completed them. 73 is n form which carried out hetero-epitaxial growth on the YSZ film 72, or the single crystal Si film of the comparatively thick (100) field of p form. The thick field oxide film by which 74 was formed on the single crystal Si film 73, and 75 are the MORT fields. 76 in the MORT field 75 is the poly silicon-gate electrode, and the SiO2 thermal-oxidation film (gate oxide film) 77 is formed between this and the single crystal Si film 73. Moreover, 78 and 79 are the source electrodes and drain electrodes by which p form or the impurity of n form is doped by high concentration.

[0085] If the main point of a manufacturing process is explained briefly, a front face will be first made pure for the single crystal Si substrate 61 of the field (100) of n form doped by high concentration by RCA washing and rare fluoric acid washing, and the YSZ film of a field (001) will be grown up all over the in 150 [nm] and the already explained high truth atmospherics beam vacuum deposition. Active oxygen annealing explained to this information-separator composite-construction object above, for example, plasma/O2 annealing, is given a little longer after growth. Then, a substrate is made immersed in the rare fluoric acid of concentration for about 10 seconds 1%, and by ultrapure water, a rinse is carried out and it dries. The front face of the YSZ film 72 of a field (100) is continuously grown epitaxially by the ordinary-pressure CVD of common knowledge of the single crystal Si of a field (100) with a thickness of 2 micrometers. Raw materials are SiCl4 and H2. Thus, the SOI substrate of a low leakage current and high dielectric-breakdown resistance is made.

[0086] Next, the 3x1013 [individual / cm2] ion implantation of the impurity B of p form is carried out all over an epitaxial Si film, and a substrate front face is made pure by RCA washing. The field oxide film 74 and the MORT field 75 are formed by the completely same LOCOS oxidation style as the above-mentioned example. While passing through a LOCOS oxidization process, in an epitaxial Si film, B impurity which carried out the ion implantation previously is diffused widely, and is activated.

[0087] After continuing, growing up the thin SiO2 thermal-oxidation film 77 (thickness 20 [nm]) which oxidizes a substrate thermally and turns into a gate oxide film to the MORT field and depositing the polysilicon contest film of thickness 300 [nm] by the LPCVD method on this further, as shown in drawing 6 , the poly silicon-gate electrode 76 is formed using a photolithography and reactive ion etching.

[0088] After removing a resist, the ion implantation of the P is carried out to a substrate front face. It is the portion except the gate electrode of the MORT field, i.e., the source, and a drain field that B is driven into an epitaxial Si film by this pouring. B is simultaneously driven also into the poly silicon-gate electrode. Acceleration voltage is 100 [keV] and a dose is 5x1015 [an individual / cm2].
[0089] In order to activate the impurity of the source electrode 78, the drain electrode 79, and the gate electrode 76 after making a substrate front face pure by RCA washing if an ion implantation is completed, the drive-in of 2 hours is performed within the diffusion furnace heated to 1120 [**]. Thus, the MOS transistor using the SOI substrate based on this invention is completed.

[Translation done.]

* NOTICES *

PRIOR ART

[Description of the Prior Art] Generally the single crystal film has the feature that many physical properties flat in crystal structure and peculiar to the material, such as eye a uniform hatchet, conductivity, a dielectric, insulation, a ferroelectricity, superconductivity nature, a semiconductor property, light-transmission nature, optical magnetic properties, and crystal periodicity, appear keenly strongly, compared with the amorphous film or the polycrystal film. Therefore, it is useful in various industrial fields, and the realization is desired strongly. In recent years, these single crystal film is loaded into Si semiconductor device or an integrated circuit, and the attempt which is going to realize the high integrated circuit and high smart device of the added value which cannot be attained only with the conventional Si system material is performed actively, and is come and required. Basic structure indispensable when such a new Si semiconductor device is constituted is the composite-construction object (the following information-separator structure and abbreviated name) of a crystalline dielectric thin film (I) and a single crystal Si (S).
[0003] When an example is given, there is a MFIS type nonvolatile random access memory cell as shown in the typical structure section view of drawing 8 . This cell replaces O portion of an MOS transistor which consists of a (Metal M)-silicon-oxide (O)-semiconductor (S) by the single crystal ferroelectric film (F) which has electrically the spontaneous polarization which can be reversed, and the single crystal dielectric film (I).
[0004] In drawing 8 , it is the single crystal oxide dielectric film (I) by which 101 was carried out at the single crystal Si substrate of a p type field (100), and hetero-epitaxial growth of 102 was carried out on the Si substrate 101, for example, (100) is the YSZ film of a field. 103 is the ferroelectric film by which hetero-epitaxial growth was carried out on the single crystal oxide dielectric film 102, for example, (001) is PbTiO3 film of a field. 104 is the gate electrode formed on the ferroelectric film 103, for example, is Pt electrode. 105 and 106 are n type source electrodes and drain electrodes, they carry out the ion implantation of P (Lynn) or the As (arsenic), respectively, make it activated by thermal diffusion, and are formed.
[0005] By this memory, information is recorded by impressing a positive or negative pulse voltage between gate (electrode G)-Si substrates (Sub), carrying out reversal fixation of the spontaneous-polarization vector of a ferroelectric film, and making a transistor into a flow or non-switch-on.
[0006] Moreover, as the above-mentioned ferroelectric layer, PbTiO3 (lead titanate) film formed by the chemical vapor growth (CVD), the magnetron sputtering method, etc., Pb(Zrx, Ti 1-x) O3 (zircon lead titanate) film, 3OBi4Ti12 (titanic-acid bismuth) film, etc. are examined (all are polarization shaft orientation single crystal films).
[0007] Moreover, as the above-mentioned single crystal dielectric layer, CeO2 (cerium oxide) film formed by the electron-beam-evaporation method or CVD, a YSZ (ITTORIYA stabilization JIRUKONIYA) film, SrTiO3 (strontium titanate) film, etc. are examined. These single crystal dielectric films are bearing a role of a buffer coat which prevents that function as a template layer for forming a single crystal ferroelectric film, and also Si substrate carries out counter diffusion to a ferroelectric.
[0008] Moreover, MFMIS structure is also proposed by the nonvolatile random access memory cell

besides the above-mentioned MFIS structure. Single crystal F layer and M layers inserted between I layers of single crystals are here, the electric conduction films, for example, Pt film etc., of a single crystal etc. information-separator structure is used for the lower part of MFM structure also in this case.
[0009] Next, the MOS transistor of the SOI structure shown in the typical structure section view of drawing 9 is also the important application of information-separator structure. The MOS transistor of this structure has the feature which should be mentioned especially that it can escape from a very detrimental latch up completely on operation.
[0010] In drawing 9 , they are single crystal dielectric films, such as CeO2 by which hetero-epitaxial growth was carried out by 111 touching Si substrate of a field (100) and 112 touching this Si substrate 111, YSZ, and SrTiO3. This Si substrate 111 and the single crystal dielectric film 112 have constituted information-separator structure. The single crystal Si layer of the p type field (100) where hetero-epitaxial growth of 113 was carried out by CVD on the single crystal dielectric film 112, the SiO2 gate oxide film in which 114 was formed by thermal oxidation of the single crystal Si layer 113, and 115 are the gate electrodes of contest polysilicon formed by CVD and dry etching on the gate oxide film 114. 116 and 117 are the source electrodes and drain electrodes of N type, they carry out the ion implantation of P (Lynn) or the As (arsenic), respectively, make it activated by thermal diffusion, and are formed.
[0011] Moreover, the oxide high-temperature superconductivity thin film wiring tried aiming at high speed processing of an integrated circuit also forms quality single crystal superconductor film (for example, YBa2Cu 3O7) wiring on information-separator structure. As I layers, YSZ and the single crystal cascade screen of Y2O3 are used, for example.
[0012] Thus, it is understood that information-separator structure is the important basic structure for realizing various devices containing the functional thin film (a ferroelectric film, a semiconductor film, an electric conduction film, a superconductivity film, dielectric film) of a single crystal on a single crystal Si substrate. However, in the present condition, the problem that a low and (3) passage-of-time destructive (TDDB) life have short (2) disruptive strengths with large (1) leakage current is in I layers of single crystal oxide dielectric thin films, and it has been a serious obstacle at realization of the above highly efficient devices.
[0013] The above-mentioned problem is explained in detail based on actual data. Drawing 7 is the leakage-current property view of a crystalline oxide dielectric thin film. It is that a characteristic curve (a) indicates the example of a property of the conventional single crystal YSZ film to be in drawing 7 . On the YSZ film of the field (100) which grew epitaxially Si substrate of an N type single crystal (100) side Leakage-current density J [A/cm2] which impressed and measured positive voltage to the gate electrode of the MIS capacity which formed and produced aluminum electrode (gate) of a diameter 200 [mum] is shown as a function of field strength Eox [V/cm]. In addition, in order to remove an absorption current component, measurement of current is performed, after carrying out voltage impression and time passes enough. Moreover, thickness is 40 [nm] and the forming-membranes method is an electron-beam-evaporation method here. The forming-membranes methods (vacuum evaporationo conditions etc.) are later mentioned in the example of this invention in the cleaning-method row of a substrate.
[0014] The leakage current of the single crystal YSZ film of the conventional example is in a very high level so that the characteristic curve (a) of drawing 7 may be seen and may be known. Considering practical use, I want to suppress leakage-current density below to J= 1 [nA/cm2] at the time of field strength Eox=1[MV/cm]. However, in the above-mentioned conventional example, this and the value which was greatly different widely are indicated to be the bases of J= 100 [muA/cm2]. Moreover, the current jump of A points in the characteristic curve (a) of drawing 7 shows that the YSZ film is carrying out dielectric breakdown on this voltage (Eox**1.5[MV/cm]). In order to apply to the above-mentioned MFIS nonvolatile memory cell etc., it is the value which cannot be said that this insulating disruptive strength is enough.
[0015] It is indispensable conditions that there is long-term dielectric-breakdown (TDDB) resistance over power supply stress in I more layers. This resistance measures and evaluates the amount Qbd of net charge [C/cm2] which passed the film by the time it generally gave and carried out dielectric breakdown of the constant-current stress to the dielectric film. The typical TDDB life when giving the constant-

current stress of J= 0.1 [mA/cm2] to the above-mentioned single crystal YSZ film was Qbd=1.2 [mC/cm2], respectively. This value is low comparable, if it compares with typical value Qbd-10[C/cm2] of thermal oxidation SiO2 film used as gate oxide films, such as an MOS transistor. In order for power supply stress to apply a YSZ film to a comparatively strong MFIS nonvolatile memory cell etc., the TDDB life of the base of at least 0.1 [C/cm2] is required.
[0016] Such a problem of I layers in information-separator structure is not having restricted to the single crystal YSZ film formed by the electron-beam-evaporation method, but is a problem by which the YSZ film produced by other single crystal oxide dielectric-materials film and other forming-membranes methods is also observed in common.

[Translation done.]

* NOTICES

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The cross section showing the basic structure of the composite-construction object based on this invention.
The cross section showing an example of the active oxygen annealer used by the manufacture method of this invention.
The cross section showing other examples of the active oxygen annealer used by the manufacture method of this invention.
The cross section showing other examples of the active oxygen annealer used by the

The cross section showing the structure of a nonvolatile memory cell as an example of the electronic device of this invention.
The cross section showing the structure which formed the MOS transistor on the SOI

The property view showing the leakage-current property of a crystalline oxide dielectric thin film.
The cross section of an example of the nonvolatile memory cell based on the conventional electronic device structure.

device structure.
[Description of Notations]
1 -- Single crystal Si substrate 2 -- Crystalline oxide dielectric film
11 -- Reactor 12 -- Vacuum pump
13 -- YSZ/Si composite-construction object in front of annealing
14 -- Susceptor 15 -- Oxygen cylinder
16 -- Ready **** 17 -- Mass flowmeter
18 -- Dielectric barrier electric discharge excimer lamp
19 -- Synthetic quartz aperture 20 -- Exhaust air bulb
21 -- Atmospheric-exhaust bulb 22 -- Evacuation equipment
31 -- Before [annealing] CeO_2/Si composite-construction object
32 -- Ozonator 33 -- Low-pressure mercury lamp
41 -- Reactor 42 -- Vacuum pump
43 -- Before [annealing] $SrTiO_3$/Si composite-construction object
44 -- Susceptor 45 -- Power electrode
46 -- Blocking capacity 47 -- Adjustment machine
48 -- RF generator 49 -- Oxygen cylinder
50 -- Ready **** 51 -- Mass flow rate controller
52 -- Exhaust air bulb 53 -- Pressure-control bulb
61 -- Si substrate 62 -- Field oxide film

[Drawing 2]
[Drawing 3]
[Drawing 4]
[Drawing 5]

manufacture

63 -- M O R T f ield 64 -- S ingle c rystal dielec tric thi n f

65 -- F e rroe le ctric f ilm 66 -- Gate e le ctrode

67 -- S ourc e e le ctrode 68 -- Drain e le ctrode

71 -- S i substrate 72 -- S ingle c rystal dielec tric thi n f

73 -- S ingle c rystal S i film 74 -- F ield oxide f ilm

75 -- M O R T f ield 76 -- The poly sil ic on-gate ele ctrode

77 -- Gate oxide film 78 -- S ourc e e le ctrode

79 -- Drain e le ctrode

[Tra ns la tion done .]

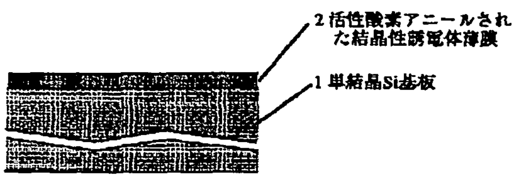
* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

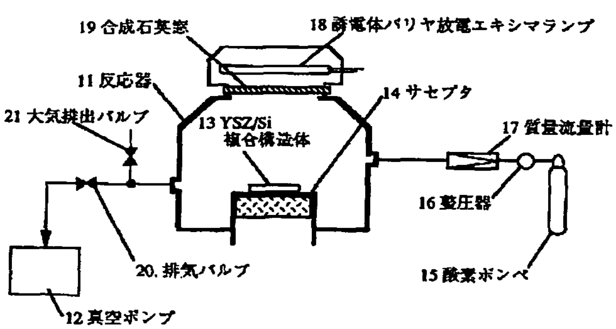
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

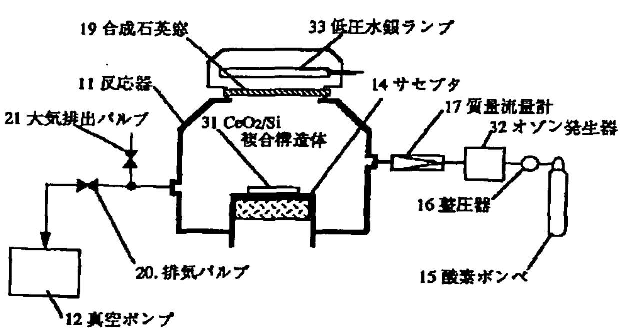
[Drawing 1]
(図1)



[Drawing 2]
(図2)

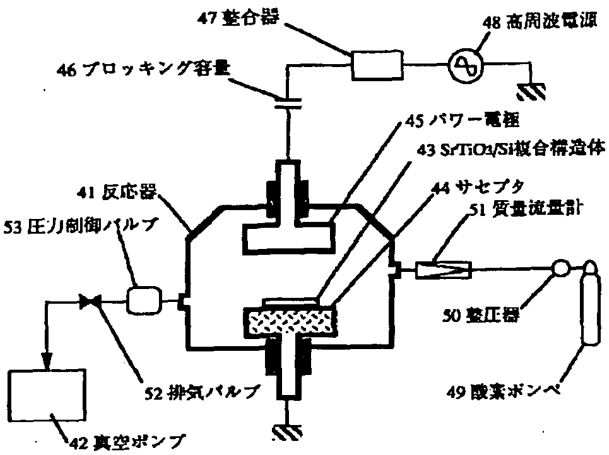


[Drawing 3]
(図3)

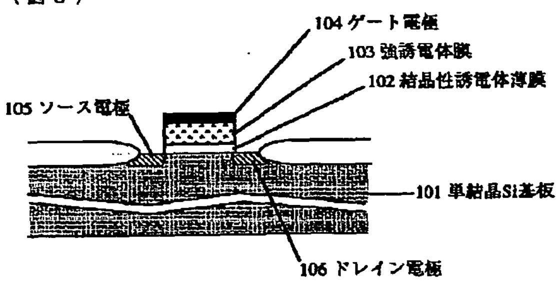


[Drawing 4]

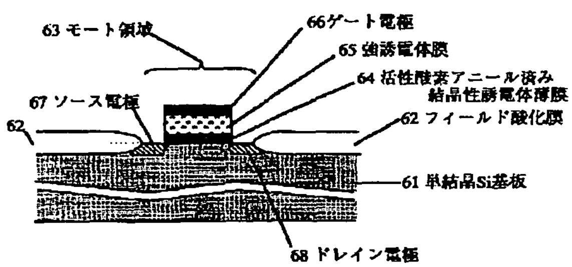
（図４）



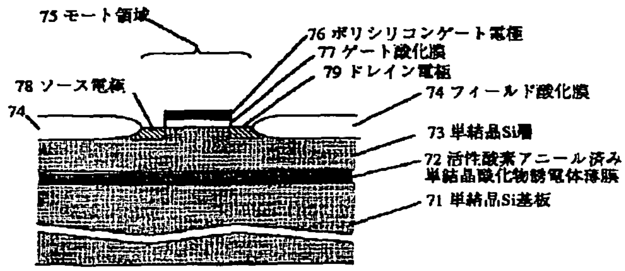
[Drawing 8]
（図８）



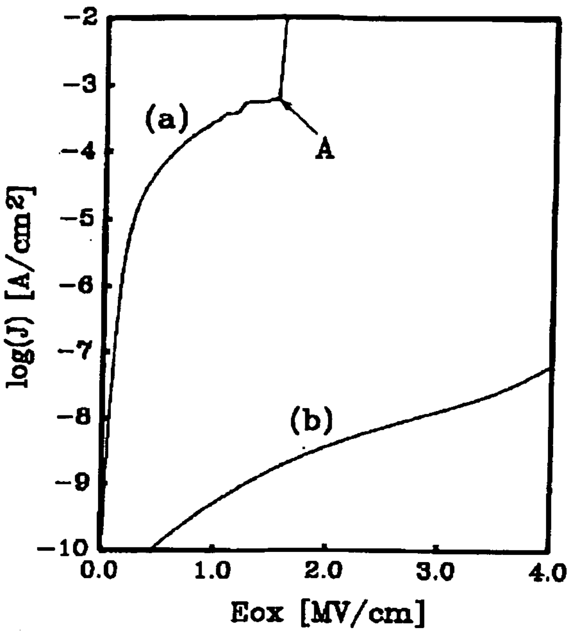
[Drawing 5]
（図５）



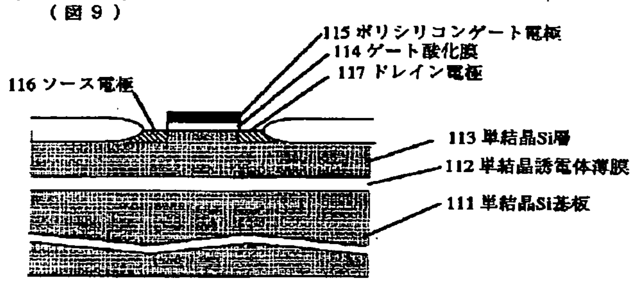
[Drawing 6]
（図６）



[Drawing 7]
(図7)



[Drawing 9]
(図9)

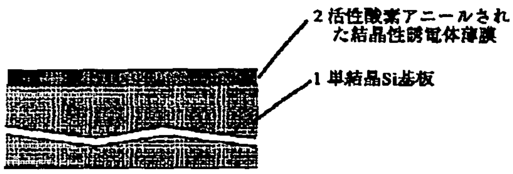


[Translation done.]

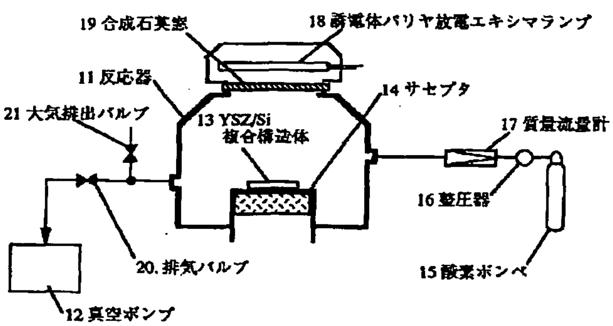
* NOTICES *

DRAWINGS

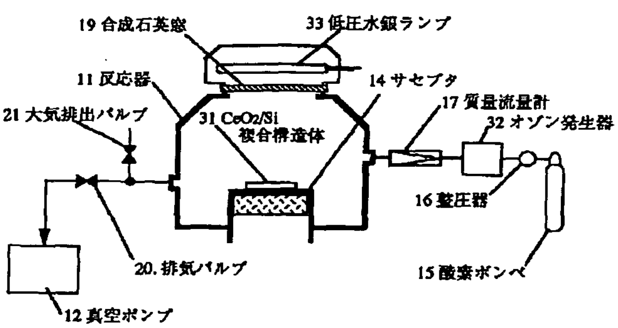
[Drawing 1]
（図１）



[Drawing 2]
（図２）

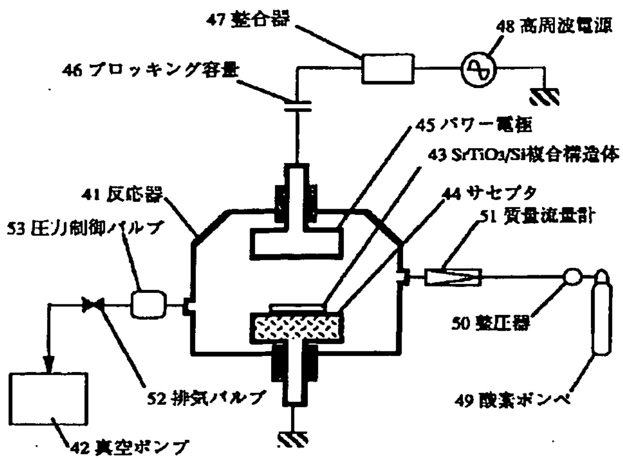


[Drawing 3]
（図３）

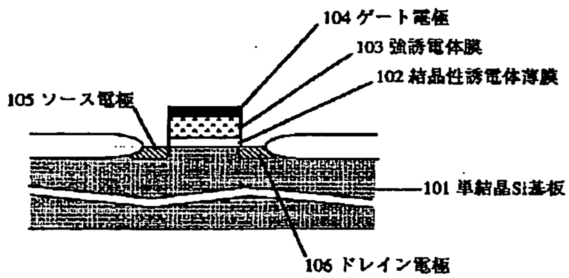


[Drawing 4]

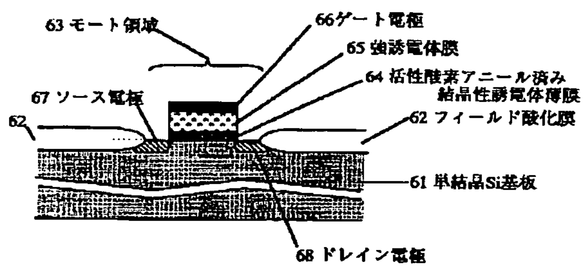
（図４）



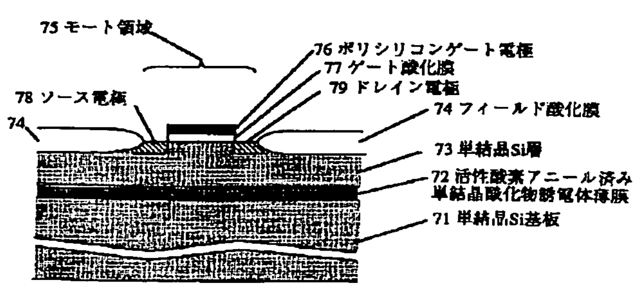
[Drawing 8]
（図８）



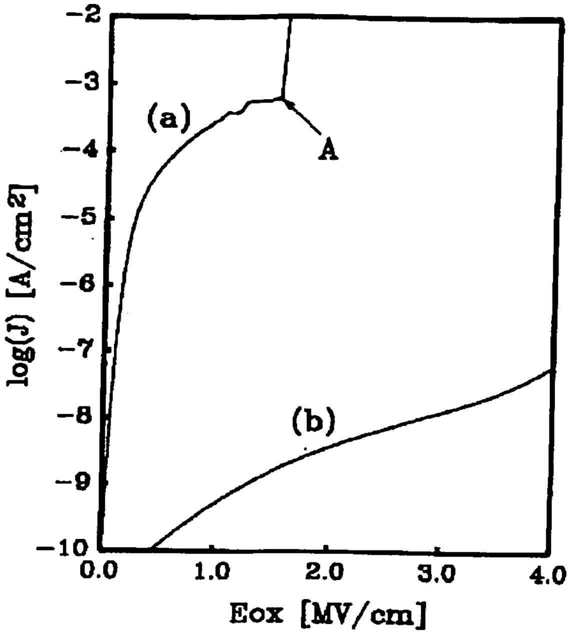
[Drawing 5]
（図５）



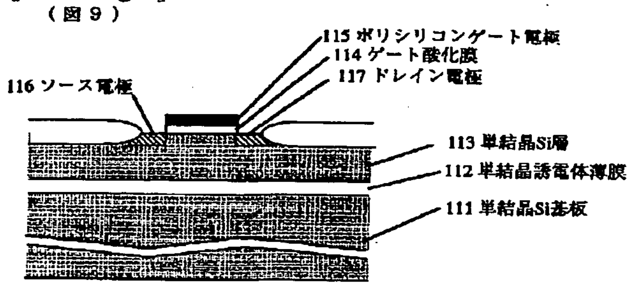
[Drawing 6]
（図６）



[Drawing 7]
（図７）



[Drawing 9]
（図９）



[Translation done.]